April 30, 2002   Product Specification

Duma Video, Inc.

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Features

- Available under terms of the SignOnce IP License
- Supports Virtex™-II devices
- 100 percent ISO/IEC 13818-2 MPEG-2-compliant elementary video stream generation
- 100 percent ISO/IEC 11172-2 MPEG-1 compliant elementary video stream generation
- 8-bit/channel pixel depths
- Standard MPEG-2 quantization entropy tables
- One input clock (74.176 MHz)
- Supports MP@ML, 422P@ML
- Standard video input interface compatible with SMPTE 274m and SMPTE 296m
- Supports 1280x720 progressive @ 59.94 frames per second
- Supports 1920x1080 interlaced @ 29.97 frames per second
- Supports chroma formats 4:2:0 and 4:2:2

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Datasheet, Design Guide
Design File Formats	EDIF Netlist
Constraints File	dumahdtvp.ucf
Verification	Testbench, test vectors
Instantiation Templates	VHDL
Reference Designs & Application Notes	None
Additional Items	Hardware demo board upon request
Simulation Tool Used	
ModelSim PE 5.5f	
Support	
Support provided by Duma Video, Inc.	

- Supports I & P frame-only encoding
- DDR SDRAM controller/interface included
- Supports 31 video quality levels
- Simple external interface
- Fully synchronous design
- Available as a fully functional and synthesizable VHDL core, including test bench files

Applications

Typical applications for the MPEG-2 HDTV encoder include video broadcast equipment, video storage, video distribution, DVD-making, and other professional video equipment.

Table 1: Core Implementation Data

Core	Supported Family	Device Tested	CLBs[1]	Clock IOBs[2]	IOBs	Performance (MHz)	Xilinx Core Tools	Special Features
HDTVp	Virtex-II	XC2V3000-5	6508	3	113	111	M4.2i	73 Block RAMs, 48 Multipliers
HDTVi	Virtex-II	XC2V3000-5	5540	2	58	111	M4.2i	73 Block RAMs, 48 Multipliers

Notes:
1. Utilization numbers for Virtex are in CLB slices
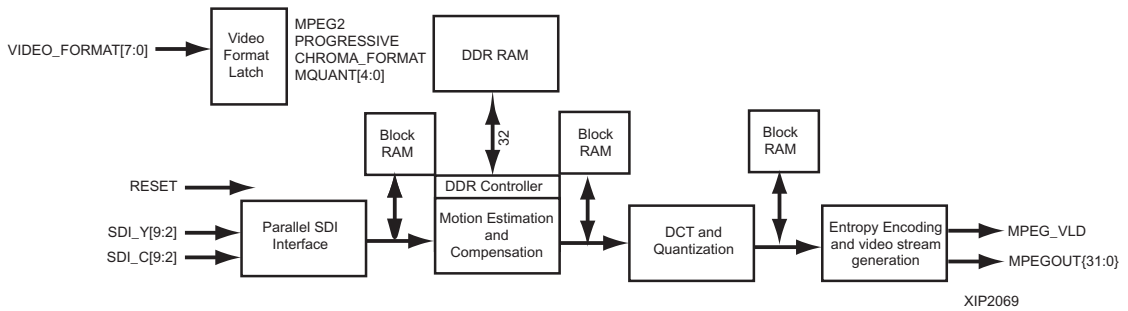2. Assuming all core I/Os are routed off-chip

Figure 1: MPEG Encoding Block Diagram

General Description

This core is a fully ISO/IEC 13818-2 compliant implementation of the MPEG-2 and 11172-2 MPEG-1 video algorithm. The simplicity of the design allows for high operational speed and makes it ideal for professional video and high-resolution real-time encoding equipment. It offers high performance and many features to meet your multimedia and digital video encoding application needs.

This core is offered in two versions. One version is targeted toward very easy implementation by processing only I frames. No external RAM is required, so a user of this core can place this core on an FPGA and start using it in an encoding system almost immediately.

The second version processes I and P frames and requires an external DDR SDRAM chip.

Functional Description

This core has five modes of operation (interlaced 4:2:2, interlaced 4:2:0, progressive 4:2:2, progressive 4:2:0, MPEG-1).

The core is designed to accelerate the video encoding process (video data extraction, motion estimation, motion compensation, DCT, quantization, and entropy encoding), which, when combined, are extremely compute intensive.

During compression, the core accepts SMPTE 274m/296m YCbCr video data. Since 1080i and 720p have the same input clock frequency (74.176 MHz), this core supports both input standards. When the "progressive" flag is High, the core accepts 720p. Otherwise, the core accepts 1080i.

This HDTV core uses three phase-aligned clocks generated from a single input clock of 74.176 MHz. The main system clock is 1.5x the HD-SDI input clock frequency (111.26 MHz). The DDR SDRAM controller uses two clocks. One clock is the system clock shifted by 180 degrees and the other is the system clock multiplied by 2x (222.52 MHz).

The DDR SDRAM controller has been specifically designed for the Micron MT46V2M32 (8MB) chip.

When "RESET" is High, the core is disabled and new video format data is latched into the core. When "RESET" goes Low, the "video_format" signal must be set. When changing the "video_format" flag, "reset" must be High for at least 500 clock cycles.

The 8-bit "video_format" flag controls the output format of the data. Each bit of the "video_format" is shown in the pinout description.

When the "chroma422" flag is High, the core outputs 422P@HL MPEG-2 elementary video stream. Otherwise, the output is MP@HL MPEG-2 elementary video stream.

The 5-bit "mquant" flag specifies the video quality of the output stream with bit 4 being the most significant bit. The higher the mquant value, the lower the quality of the video, but higher the compression ratio. For example, mquant equal to the integer value 8 is average quality. A value of 1 is near lossless video and a value of 31 is very low-quality video. An mquant value of 0 is prohibited.

The core is pipelined with each stage ending in block RAMs as shown in Figure 1. The first stage extracts the active video data, then stores that data in the block RAMs.

The motion estimation/compensation stage compares the previous frame of video stored in DDR RAM with the current frame. The output is stored in the next set of block RAMs.

The DCT/quantization stage performs a discrete cosine transform and MPEG quantization using the standard MPEG-2 quantization tables. It then passes the quantized data to the next set of block RAMs.

The entropy encoder zigzag scans the macroblocks and encodes the data using the standard MPEG-2 Huffman tables. The entropy encoder also generates all the necessary MPEG-2 headers for the video bit stream. The output is a 32-bit word that is the elementary video stream. When "MPEG_VLD" is High, the 32-bit data is valid. This output can go directly into a FIFO, PCI interface, SCSI, or other synchronous output. In our simulations, we output the data into a FIFO, then a PCI interface. Duma Video can provide a FIFO, if needed.

Core Modifications

Potential core modifications:

- All quantization and encoding tables are fixed but can be modified upon the user's request
- Integrating the SDI serial-to-parallel converter into our core
- Integrating a PCI interface
- Full search motion estimation
- Extracting, compressing, and encoding audio data multiplexed in the incoming video data. The final stream a core would generate is a packetized elementary stream ("PES").
- Variable Group of Pictures ("GOP") structure
- 10-bit video; current core uses 8-bit video
- Addition of 1080p (1920x1080 @ 59.94fps)

The flexibility of our core allows us to implement all MPEG encoding, including the audio, on a single FPGA, or just certain requirements. Please contact Duma Video for further information.

Pin Description

The pin signal names are shown in Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
CLK_SDI	Input	Video input Clock
CLK_SYS	Input	System Clock
CLK_SYS2x	Input	DDR SDRAM Controller clock
SDI_Y[9:2]	Input	HD-SDI Luma Values conforming to SMPTE 274m/296m
SDI_C[9:2]	Input	HD-SDI Chroma Values
RESET	Input	Reset, Active High
VIDEO_FORMAT [7:0]	Input	Controls the output format. Default is "00001000". Prohibited codes are: "---00000", "10------", "111-----"
VIDEO_FORMAT [7]	Input	High: MPEG-1 Low: MPEG-2
VIDEO_FORMAT [6]	Input	High: Progressive, 720p @ 59.94 fps Low: Interlaced, 1080i @ 29.97 fps
VIDEO_FORMAT [5]	Input	High: Chroma 4:2:2 Low: Chroma 4:2:0
VIDEO_FORMAT [4:0]	Input	MQUANT integer value [1-31]
MPEG_VLD	Output	MPEG encoded data is valid
MPEGOUT[31:0]	Output	MPEG encoded output data
DDR_xxx[54:0]	I/O	DDR SDRAM I/O

Core Assumptions

- GOP structure is 15 frames
- The same mquant value is used for I and P frames
- Time code always starts at 00:00:00:00 after a reset
- Interlaced I frames are always encoded using the MPEG-2 VLC_format look up tables and alternate scan

Verification Methods

Multiple video streams of 1080i and 720p video data were input into our core to generate MPEG-2 elementary video streams ("EVS"). The EVS were verified by playing the generated streams in multiple MPEG-2 players.

Recommended Design Experience

Good knowledge of the ISO/IEC 13818-2 and 11172-2 specifications, as well as terminology, is recommended. Users should be familiar with VHDL synthesis and simulation and Xilinx design flows, as well.

Ordering Information

The MPEG-2 HDTV Encoder core is provided under license by AllianceCORE partner Duma Video for use in Xilinx programmable logic devices as an AllianceCORE product under terms of the SignOnce IP license.

An RTL synthesizable source code is also available.

Please contact Duma Video for information about pricing and additional information about this AllianceCORE product.

Duma Video reserves the right to change any specification detailed in this document at any time without notice, and assumes no responsibility for any error in this document.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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