American National Standard

for Information Technology –

AT Attachment with Packet Interface Extensions 5 (ATA/ATAPI-5)

Corrected: Secretariat: Information Technology Industry Council

Page 116 of NCITS 340-2000 ATA/ATAPI-5 clause 8.13.46 was not properly transcribed from proposal t13/d01127r0. The wording is modified to conform with the approved proposal.

Page 265 through 270 of NCITS 340-2000 clause 9.8 was not properly converted from the flow charts in NCITS 317-1998 to the state diagrams. The state diagrams figures 33 and 34 and the associated text is modified to indicate that the device interrupts only at command completion.

Page 280 of NCITS 340-2000 clause 9.12 the behavior of setting the signature for the IDENTIFY DEVICE and READ SECTOR(S) commands did not agree with the command descriptions in clause 8. The wording is modified to agree with clause 8.

Page 306 of NCITS 340-2000 figure 54 the initial states shown for STOP and HSTROBE were incomplete and the released state of DDMARDY- was incorrect. The figure is corrected to represent the actual states.

Page 309 and 310 of NCITS 340-2000 figures 57 and 58 the ending states shown for STOP and HSTROBE were incomplete and the released state of DDMARDY- was incorrect. The figure is corrected to represent the actual states.

Page 321 of NCITS 340-2000 figure A.8 the dimension A8 is drawn from the top of the well to the detent the same as dimension A10. The figure is corrected to show dimension A8 from the top of the well to the bottom of the well.

Page 380 of NCITS 340-2000 figure F.1 the entries marked “A” did not have an “*” included when the entry was modified due to proposal T13/e99126r0. The table is corrected to rlfect the addition of the “*”.

Page 382 of NCITS 340-2000 figure F.3 the entries in the “ PKT fea” columns for MEDIA EJECT, MEDIA LOCK, MEDIA UNLOCK, READ NATIVE MAX ADDRESS, SERVICE, SET MAX ADDRESS, and the SMART commands do not agree with the feature set description of the command descriptions in clause 8. The wording is modified to agree with clause 8.

In this erratum, pages 116,265, 266, 267, 268, 269, 270, 280,306,309,310,321, 380 and 382 are reprinted with corrections.

8.13.34 Word 75: Queue depth

Bits 4 through 0 of word 75 shall have the content described for word 75 of the IDENTIFY DEVICE command.

8 13 35 Words 76-79: Reserved

8.13.36 Word 80: Major revision number

Word 80 shall have the content described for word 80 of the IDENTIFY DEVICE command.

8.13.37 Word 81: Minor revision number

Word 81 shall have the content described for word 81 of the IDENTIFY DEVICE command.

8.13.38 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall have the content described for words 82, 83, and 84 of the IDENTIFY DEVICE command except that bit 4 of word 82 shall be set to one.

8.13.39 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall have the content described for words 85, 86, and 87 of the IDENTIFY DEVICE command except that bit 4 of word 85 shall be set to one.

8.13.40 Word 88:Ultra DMA modes

Word 88 shall have the content described for word 88 of the IDENTIFY DEVICE command.

8.13 41 Word 89: Time required for Security erase unit completion

Word 89 shall have the content described for word 89 of the IDENTIFY DEVICE command.

8.13.42 Word 90: Time required for Enhanced security erase unit completion

Word 90 shall have the content described for word 90 of the IDENTIFY DEVICE command.

8.13.43 Word 91-92: Reserved

8.13.44 Word 93: Hardware reset results

Word 93 shall have the content described for word 93 of the IDENTIFY DEVICE command.

8.13.45 Word 94-125: Reserved

8.13.46 Word 126: ATAPI byte count=0 behavior

If the contents of word 126 are 0000h and the byte count limit is cleared to zero, the device shall return command aborted.

If the contents of word 126 are non-zero and the byte count limit is set to zero, the device shall use the contents of word 126 as the actual byte count limit for the current command and shall not abort.

The device may be reconfigured to report a new value. However, after the device is reconfigured, the content of word 126 reported shall not change until after the next hardware reset or power-on reset event.

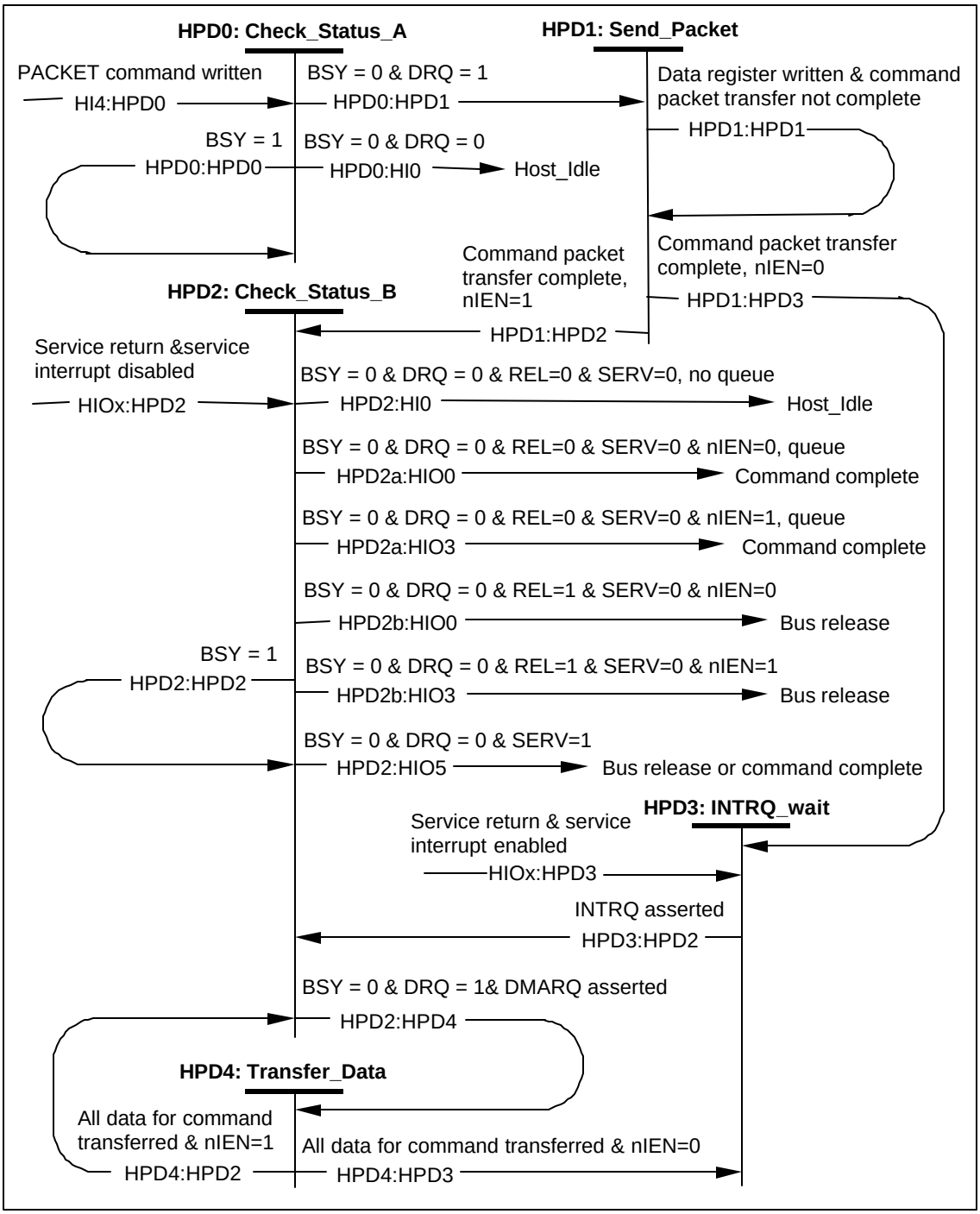


Figure 33 - Host PACKET DMA command state diagram

HPD0: Check_Status_A State: This state is entered when the host has written a PACKET command to the device.

When in this state, the host shall read the device Status register. When entering this state from the HI4 state, the host shall wait 400 ns before reading the Status register.

Transition HPD0:HPD0: When BSY is set to one, the host shall make a transition to the HPD0: Check_Status_A state.

Transition HPD0:HPD1: When BSY is cleared to zero and DRQ is set to one, then the host shall make a transition to the HPD1: Send_Packet state.

Transition HPD0:HI0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, and SERV is cleared to zero, then the command is completed and the host shall make a transition to the HI0: Host_Idle state (see figure 19). If an error is reported, the host shall perform appropriate error recovery.

HPD1: Send_Packet State: This state is entered when BSY is cleared to zero, DRQ is set to one.

When in this state, the host shall write a byte of the command packet to the Data register.

Transition HPD1:HPD1: When the Data register has been written and the writing of the command packet is not completed, the host shall make a transition to the HPD1: Send_Packet state.

Transition HPD1:HPD2: When the Data register has been written, the writing of the command packet is completed, and nIEN is set to one, the host shall make a transition to the HPD2: Check_Status_B state.

Transition HPD1:HPD3: When the Data register has been written, the writing of the command packet is completed, and nIEN is cleared to zero, the host shall make a transition to the HPD3: INTRQ wait state.

HPD2: Check_Status_B State: This state is entered when the host has written the command packet to the device, when INTRQ has been asserted, when a DRQ data block has been transferred, or from a service return when the service interrupt is disabled.

When in this state, the host shall read the device Status register. When entering this state from the HPD1 or HPD4 state, the host shall wait one PIO transfer cycle time before reading the Status register. The wait may be accomplished by reading the Alternate Status register and ignoring the result.

Transition HPD2:HPD2: When BSY is set to one, and DRQ is cleared to zero, the host shall make a transition to the HPD2: Check_Status_B state.

Transition HPD2:HPD4: When BSY is cleared to zero, DRQ is set to one, and DMARQ is asserted, then the host shall make a transition to the HPD4: Transfer_Data state. The host shall have set up the DMA engine before this transition.

Transition HPD2:HI0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, and the device queue is empty, then the command is completed and the host shall make a transition to the HI0: Host_Idle state (see figure 19). If an error is reported, the host shall perform appropriate error recovery.

Transition HPD2a:HIO0: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is cleared to zero, and the device has a queue of released commands, then the command is completed and the host shall make a transition to the HIO0: Command completed state (see figure 19). If an error is reported, the host shall perform appropriate error recovery.

Transition HPD2a:HIO3: When BSY is cleared to zero, DRQ is cleared to zero, REL is cleared to zero, SERV is cleared to zero, nIEN is set to one, and the device has a queue of released commands, then the command is completed and the host shall make a transition to the HIO3: Command completed state (see **Error! Reference source not found.**). If an error is reported, the host shall perform appropriate error recovery.

Transition HPD2b:HIO0: When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero, and nIEN is cleared to zero, then the host shall make a transition to the HIO0: INTRQ_wait_A state (see figure 20). The bus has been released.

Transition HPD2b:HIO3: When BSY is cleared to zero, DRQ is cleared to zero, REL is set to one, SERV is cleared to zero, and nIEN is set to one, then the host shall make a transition to the HIO3: Check_status_A state (see figure 20). The bus has been released.

Transition HPD2:HIO5: When BSY is cleared to zero, DRQ is cleared to zero, and SERV is set to one, then the host shall make a transition to the HIO5: Write_SERVICE state (see figure 20). The command is completed or the bus has been released, and another queued command is ready for service. If an error is reported, the host shall perform appropriate error recovery.

HPD3: INTRQ_Wait State: This state is entered when the command packet has been transmitted, when a service return is issued and the service interrupt is enabled, or when the command has completed, and nIEN is cleared to zero.

When in this state, the host shall wait for INTRQ to be asserted.

Transition HPD3:HPD2: When INTRQ is asserted, the host shall make a transition to the HPD2: Check_Status_B state.

HPD4: Transfer_Data State: This state is entered when BSY is cleared to zero, DRQ is set to one, and DMARQ is asserted.

When in this state, the host shall read or write the device Data port to transfer data. If the bus has been released, the host shall read the Sector Count register to determine the Tag for the queued command to be executed.

Transition HPD4:HPD2: When all data for the request has been transferred and nIEN is set to one, then the host shall make a transition to the HPD2: Check_Status_B state.

Transition HPD4:HPD3: When all data for the request has been transferred and nIEN is cleared to zero, then the host shall make a transition to the HPD3: INTRQ_wait state.

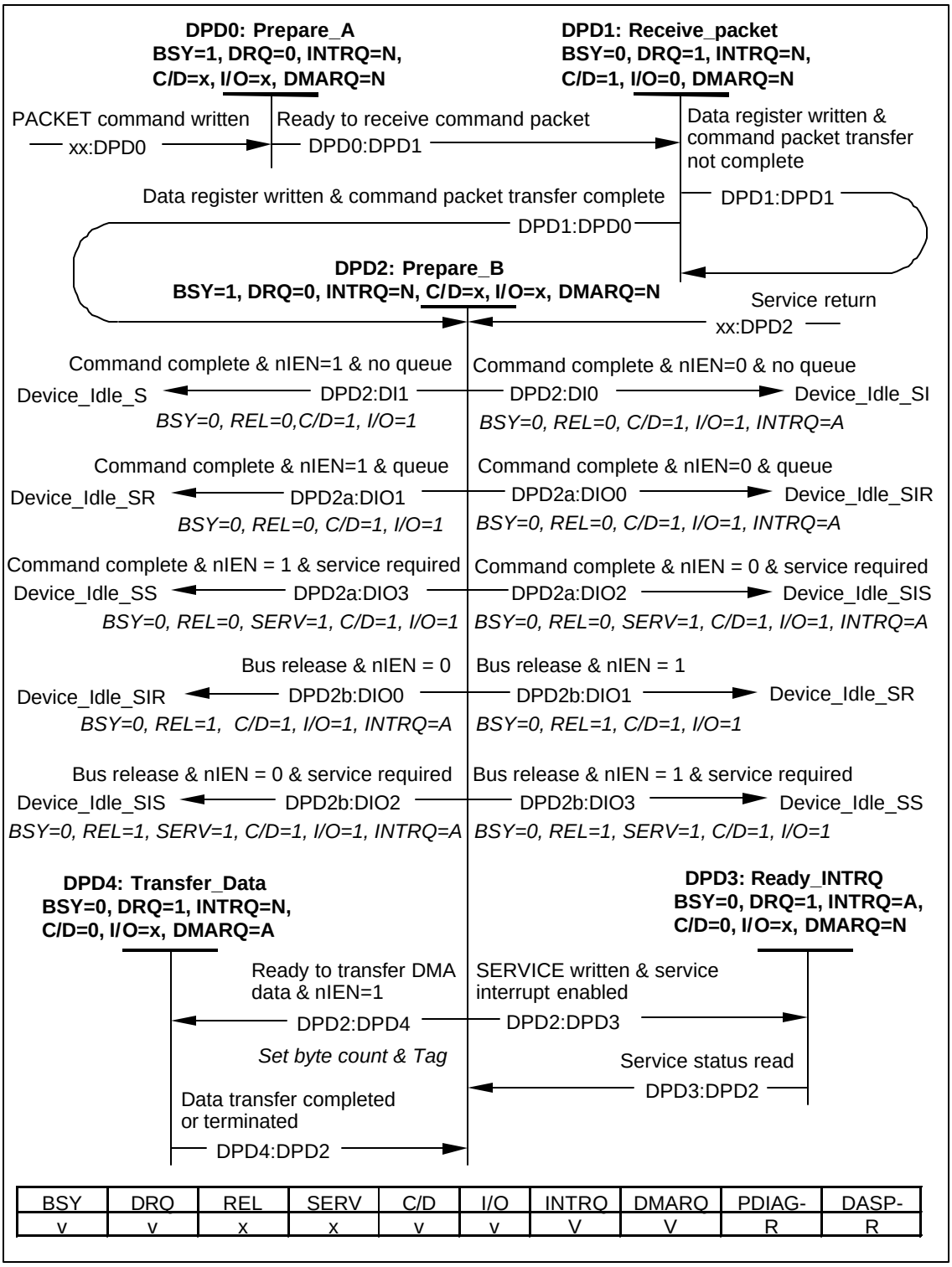


Figure 34 - Device PACKET DMA command state diagram

DPD0: Prepare_A State: This state is entered when the device has a PACKET written to the Command register.

When in this state, device shall set BSY to one, clear DRQ to zero, and negate INTRQ within 400 ns of the receipt of the command and shall prepare to receive a command packet. If the command is a queued command, the device shall verify that the Tag is valid.

Transition DPD0:DPD1: When the device is ready to receive the command packet for a command, the device shall make a transition to the DPD1: Receive_Packet state.

DPD1: Receive_Packet State: This state is entered when the device is ready to receive the command packet.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is set to one, I/O is cleared to zero, and REL is cleared to zero. When in this state, the device Data register is written.

Transition DPD1:DPD1: If the Data register is written and the entire command packet has not been received, then the device shall make a transition to the DPD1: Receive_Packet state.

Transition DPD1:DPD2: When the Data register is written and the entire command packet has been received, then the device shall make a transition to the DPD2: Prepare_B state.

DPD2: Prepare_B State: This state is entered when the command packet has been received or from a Service return.

When in this state, device shall set BSY to one, clear DRQ to zero, and negate INTRQ. The device shall check for errors, determine if the data transfer is complete, and if not, prepare to transfer the DMA data.

If the command is overlapped and the release interrupt is enabled, the device shall bus release as soon as the command packet has been received.

Transition DPD2:DPD4: When the device is ready to transfer DMA data for a command and nIEN is set to one, then the device shall set the command Tag and byte count, set the interrupt pending, and make a transition to the DPD4: Transfer_Data state.

Transition DPD2:DPD3: When the service interrupt is enabled and the device has SERVICE written to the Command register, then the device shall set the command Tag and byte count and make a transition to the DPD3: Ready_INTRQ state.

Transition DPD2:DI0: When the command has completed or an error occurs that causes the command to abort, the device has no other command released, and nIEN is cleared to zero, then the device shall set the interrupt pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and make a transition to the DI0: Device_Idle_SI state (see figure 21).

Transition DPD2:DI1: When the command has completed or an error occurs that causes the command to abort, the device has no other command released, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and make a transition to the DI1: Device_Idle_S state (see figure 21).

Transition DPD2a:DIO0: When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service, and nIEN is cleared to zero, then the device shall set the interrupt pending, set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and make a transition to the DIO0: Device_Idle_SIR state (see figure 22).

Transition DPD2a:DIO1: When the command has completed or an error occurs that causes the command to abort, the device has another command released but not ready for service, and

nIEN is set to one, then the device shall, set appropriate error bits, set C/D and I/O to one, clear BSY to zero, and make a transition to the DIO1: Device_Idle_SR state (see figure 22).

Transition DPD2a:DIO2: When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service, and nIEN is cleared to zero, then the device shall set the interrupt pending, set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero, and make a transition to the DIO2: Device_Idle_SIS state (see figure 22).

Transition DPD2a:DIO3: When the command has completed or an error occurs that causes the command to abort, the device has another command ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set SERV to one, clear BSY to zero, and make a transition to the DIO3: Device_Idle_SS state (see figure 22).

Transition DPD2b:DIO0: When the command is released and nIEN is cleared to zero, then the device shall set the interrupt pending, set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero, and make a transition to the DIO0: Device_Idle_SIR state (see figure 22).

Transition DPD2b:DIO1: When the command is released and nIEN is set to one, then the device shall, set appropriate error bits, set C/D and I/O to one, set REL to one, clear BSY to zero, and make a transition to the DIO1: Device_Idle_SR state (see figure 22).

Transition DPD2b:DIO2: When the is released, the device has another command ready for service, and nIEN is cleared to zero, then the device shall set the interrupt pending, set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero, and make a transition to the DIO2: Device_Idle_SIS state (see figure 22).

Transition DPD2b:DIO3: When the command is released, the device has another command ready for service, and nIEN is set to one, then the device shall set appropriate error bits, set C/D and I/O to one, set REL to one, set SERV to one, clear BSY to zero, and make a transition to the DIO3: Device_Idle_SS state (see figure 22).

DPD3: Ready_INTRQ State: This state is entered to interrupt upon receipt of a SERVICE command when service interrupt is enabled.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is asserted, C/D is cleared to zero, and I/O is set to one for PIO data-out or cleared to zero for PIO data-in.

Transition DPD3:DPD2: When the Status register is read to respond to a service interrupt, the device shall make a transition to the DPD2: Prepare_B state.

DPD4: Data_Transfer State: This state is entered when the device is ready to transfer DMA data.

When in this state, BSY is cleared to zero, DRQ is set to one, INTRQ is negated, C/D is cleared to zero, I/O is set to one for data-out or cleared to zero for data-in, DMARQ is asserted, and data is transferred as described in Multiword DMA timing or Ultra DMA protocol.

Transition DPD4:DPD2: When the data transfer has been completed, then the device shall make a transition to the DPD2: Prepare_B state.

9.9 READ/WRITE DMA QUEUED command protocol

This class includes:

DDR1: Set_status State: This state is entered when the device has released the bus and set BSY to one.

When in this state the device should stop execution of any uncompleted command. The device should end background activity (e.g., immediate commands, see MMC and MMC-2).

The device should not revert to the default condition. If the device reverts to the default condition, the device shall report an exception condition by setting CHK to one in the Status register. MODE SELECT conditions shall not be altered.

The device shall set the signature values (see 9.12). The content of the Features register is undefined.

The device shall clear bit 7 in the ERROR register to zero. The device shall clear bits 6, 5, 4, 3, 2, and 0 in the Status register to zero.

Transition DDR1:DI1: When the status has been set, the device shall clear BSY to zero and make a transition to the DI1: Device_idle_S state (see Figure 21).

9.12 Signature and persistence

A device not implementing the PACKET command feature set shall place the signature in the Command Block registers listed below for power-on reset, hardware reset, software reset, and the EXECUTE DEVICE DIAGNOSTIC command.

If the device does not implement the PACKET command feature set, the signature shall be:

Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	00h

A device implementing the PACKET command feature set shall place the signature in the Command Block registers listed below for power-on reset, hardware reset, software reset, the EXECUTE DEVICE DIAGNOSTIC command, and the DEVICE RESET command. The DEVICE RESET command shall not change the value of the DEV bit when writing the signature into the Device/Head register for a device implementing the PACKET command feature set. If the device implements the PACKET command feature set, the signature is also written in the registers for the IDENTIFY DEVICE and READ SECTOR(S) commands.

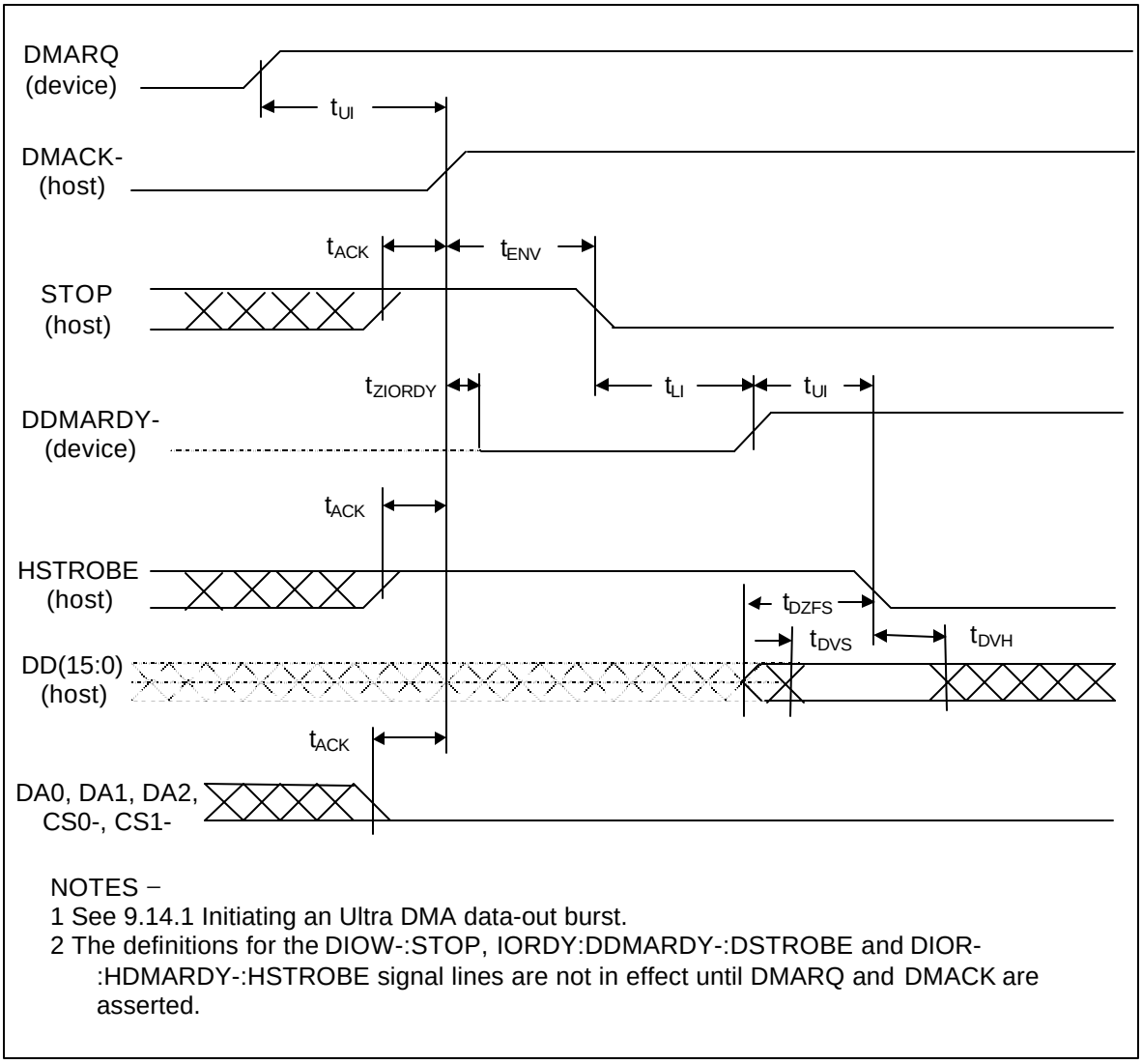
If the device implements the PACKET command feature set, the signature shall be:

Sector Count	
Sector Number	
Cylinder Low	
Cylinder High	
Device/Head	000x0000b where x equals 0 except when responding to a DEVICE RESET, IDENTIFY DEVICE, or READ SECTOR(S) command. For the DEVICE RESET, IDENTIFY DEVICE, or READ SECTOR(S) command the value of x is not changed from that existing when the command is written to the Command register.

If the PACKET command feature set is implemented by a device, then the signature values written by the device in the Command Block registers following power-on reset, hardware reset, software reset, or the DEVICE RESET command shall not be changed by the device until the device receives a command that sets DRDY to one. Writes by the host to the Command Block registers that contain the signature values shall overwrite the signature values and invalidate the signature.

10.2.4.6 Initiating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.

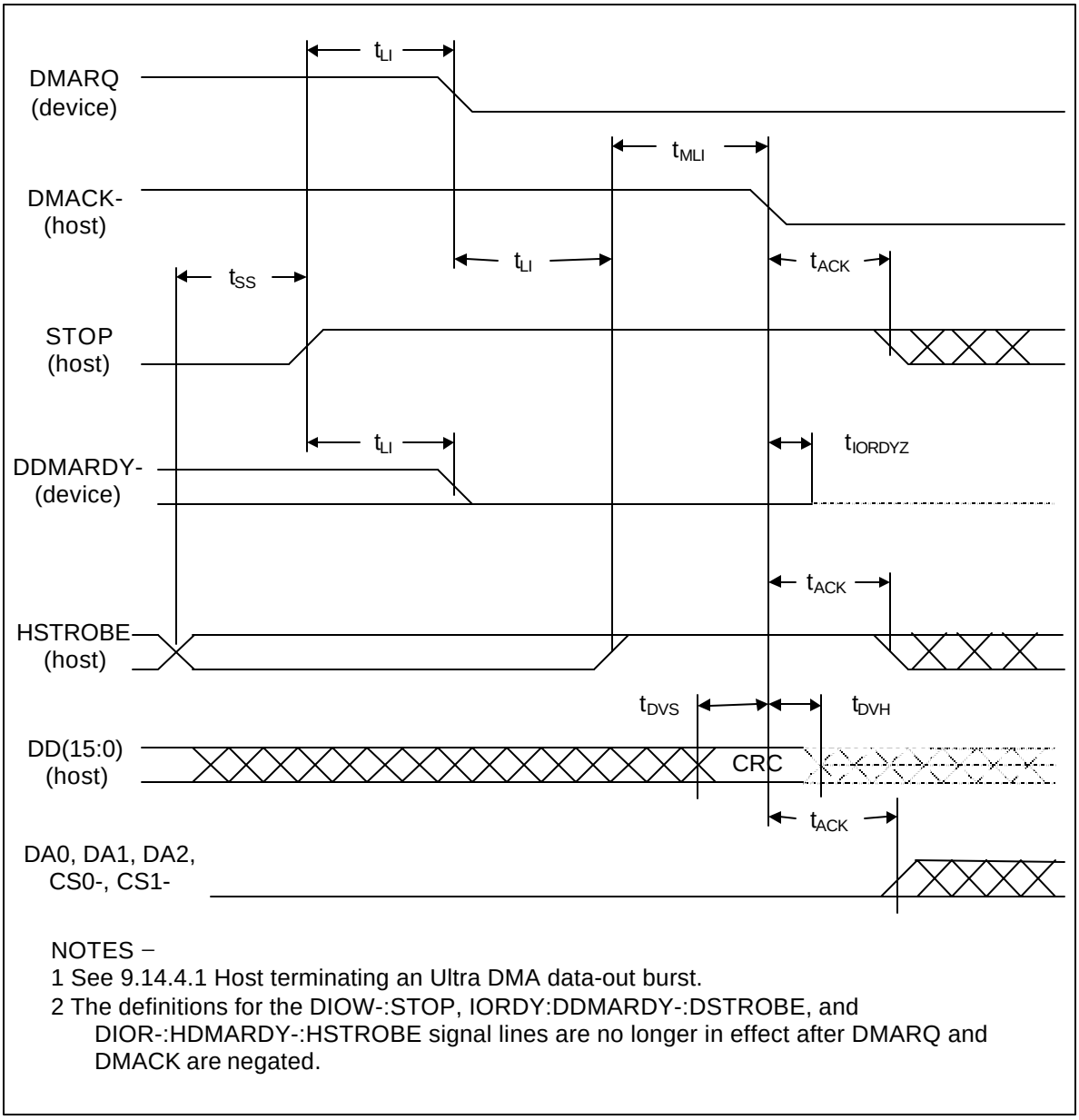


NOTES –
1 See 9.14.1 Initiating an Ultra DMA data-out burst.
2 The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE and DIOR-:HDMARDY-:HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 54 – Initiating an Ultra DMA data-out burst

10.2.4.9 Host terminating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in 10.2.4.

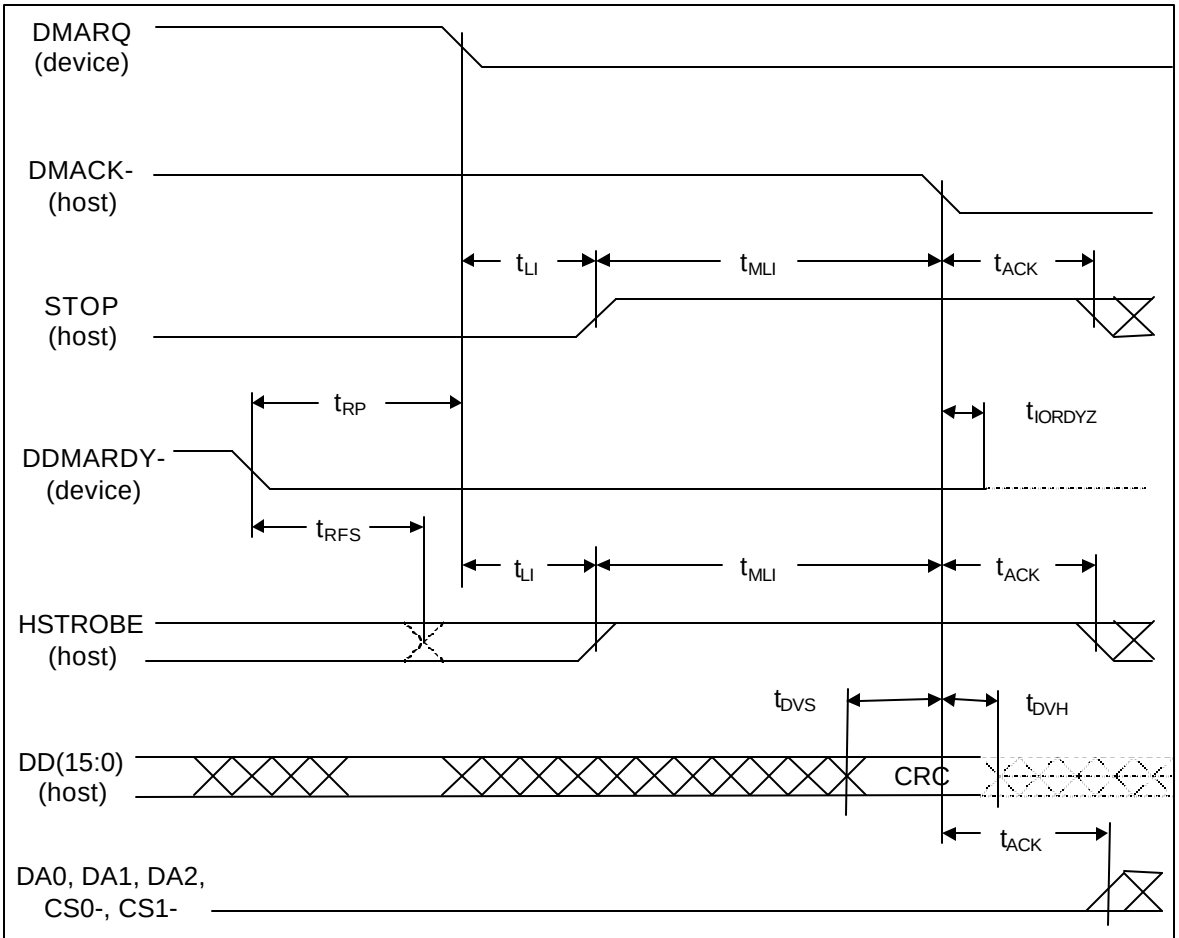


NOTES –
1 See 9.14.4.1 Host terminating an Ultra DMA data-out burst.
2 The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE, and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 57 – Host terminating an Ultra DMA data-out burst

10.2.4.10 Device terminating an Ultra DMA data-out burst

The values for the timings for each of the Ultra DMA modes are contained in10.2.4.



NOTES –
1 See 9.14.4.2 Device pausing an Ultra DMA data-out burst.
2 The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE, and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 58 – Device terminating an Ultra DMA data-out burst

A.2 4-pin power connector

The power connector is a 4-pin connector. The header mounted to a device is shown in figure A.8 and the dimensions are shown in table A.10. The connector mounted to the end of the cable is shown in figure A.9 and the dimensions are shown in table A.11. Pin assignments for these connectors are shown in table A.12.

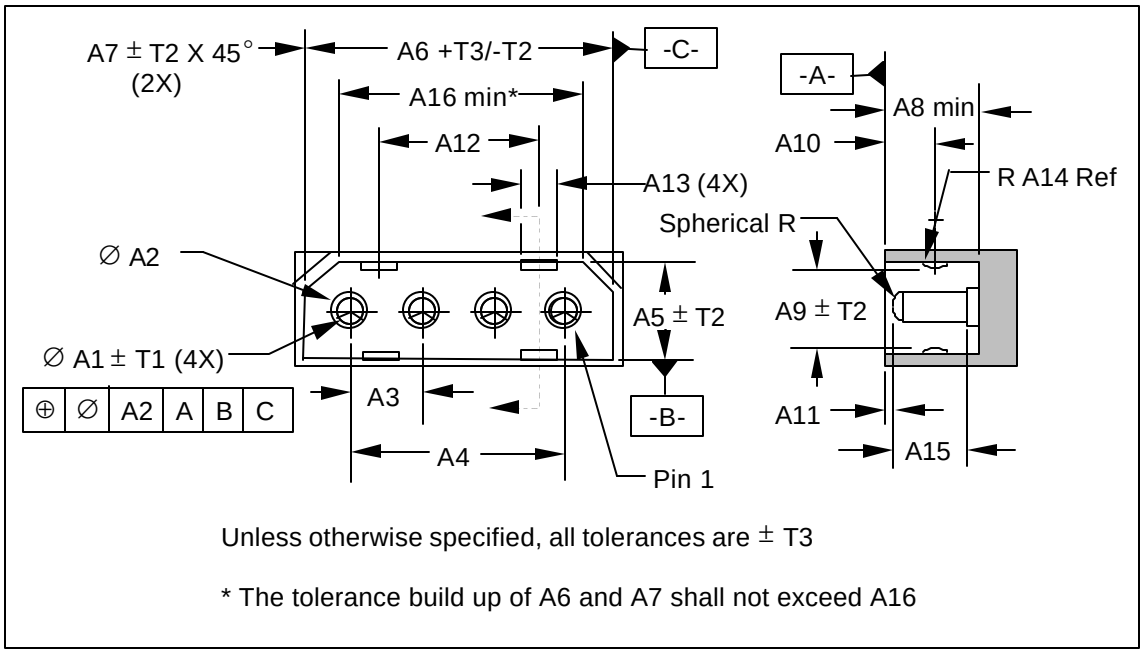


Figure A.8 – Device 4-pin power header

Table A.10 – Device 4-pin power header

Dimension	Millimeters	Inches
A 1	2.10	0.083
A 2	3.50	0.138
A 3	5.08	0.200
A 4	15.24	0.600
A 5	6.60	0.260
A 6	21.32	0.839
A 7	1.65	0.065
A 8	7.50	0.295
A 9	6.00	0.236
A 10	4.95	0.195
A 11	1.00	0.039
A 12	11.18	0.440
A 13	3.80	0.150
A 14	3.00	0.118
A 15	5.10	0.201
A 16	17.80	0.701
T 1	0.04	0.0016
T 2	0.15	0.006
T 3	0.25	0.010

Annex F
(informative)
Command set summary

The following four tables are provided to facilitate the understanding of the command set. Table F.1 provides information on which command codes are currently defined. Table F.2 provides a list of all of the commands in order of command code. Table F.3 provides a summary of all commands with the protocol, required use, command code, and registers used for each. Table F.4 shows the status and error bits used by each command.

Table F.1 – Command matrix

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	C	R	R	C	R	R	R	R	C	R	R	R	R	R	R	R
1x	O	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
2x	C	O*	O	O	R	R	R	R	R	R	R	R	R	R	R	R
3x	C	O*	O	O	R	R	R	R	C	R	R	R	O	R	R	R
4x	C	O*	R	R	R	R	R	R	R	R	R	R	R	R	R	R
5x	O	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
6x	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
7x	C	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
8x	V	V	V	V	V	V	V	F	V	V	V	V	V	V	V	V
9x	C	C	C	R	E	E	E	E	E	E	V	R	R	R	R	R
Ax	C	C	C	R	R	R	R	R	R	R	R	R	R	R	R	R
Bx	C	R	R	R	R	R	R	R	A*	A*	A*	A*	A*	A*	A*	A*
Cx	F	V	V	V	C	C	C	C	C	O*	C	O*	C	C	R	R
Dx	R	R	R	R	R	R	R	R	R	R	C	E	E	E	C	C
Ex	C	C	C	C	C	C	C	C	C	E	R	R	C	C	O	C
Fx	V	C	C	C	C	C	C	V	C	C	V	V	V	V	V	V

Key:
C = a defined command.
R = Reserved, undefined in current specifications.
V = Vendor specific commands.
O = Obsolete.
E=a retired command.
F=If the device does not implement the CFA feature set, this command code is Vendor specific.
A=Reserved for assignment by the CompactFlash™ Association
* indicates that the entry in this table has changed from ATA/ATAPI-4, NCITS 317-1998.

Table F.3 – Command codes and parameters

proto	Command	typ	PKT fea	Command code	Parameters used				
					FR	SC	SN	CY	DH
ND	CFA ERASE SECTORS	O	N	C0h		y	y	y	y
ND	CFA REQUEST EXTENDED ERROR	O	N	03h					D
PI	CFA TRANSLATE SECTOR	O	N	87h			y	y	y
PO	CFA WRITE MULTIPLE W/OUT ERASE	O	N	CDh		y	y	y	y
PO	CFA WRITE SECTORS W/OUT ERASE	O	N	38h		y	y	y	y
ND	CHECK POWER MODE	M	M	E5h		y			D
DR	DEVICE RESET	O	M	08h					D
PO	DOWNLOAD MICROCODE	O	N	92h	y	y	y	y	D
DD	EXECUTE DEVICE DIAGNOSTIC	M	M	90h					D*
ND	FLUSH CACHE	M	M	E7h		y	y	y	y
ND	GET MEDIA STATUS	O	O	DAh					D
PI	IDENTIFY DEVICE	M	N	ECh					D
PI	IDENTIFY PACKET DEVICE	N	M	A1h					
ND	IDLE	M	O	E3h		y			D
ND	IDLE IMMEDIATE	M	M	E1h					D
ND	INITIALIZE DEVICE PARAMETERS	M	N	91h		y			y
ND	MEDIA EJECT	O	N	EDh					D
ND	MEDIA LOCK	O	N	DEh					D
ND	MEDIA UNLOCK	O	N	DFh					D
ND	NOP	O	M	00h					D
P	PACKET	N	M	A0h	y	y	y	y	D
PI	READ BUFFER	O	N	E4h					D
DM	READ DMA	M	N	C8h		y	y	y	y
DMO	READ DMA QUEUED	O	N	C7h	y	y	y	y	y
PI	READ MULTIPLE	M	N	C4h		y	y	y	y
ND	READ NATIVE MAX ADDRESS	O	O	F8h					D
PI	READ SECTOR(S)	M	N	20h		y	y	y	y
ND	READ VERIFY SECTOR(S)	M	N	40h		y	y	y	y
PO	SECURITY DISABLE PASSWORD	O	O	F6h					D
ND	SECURITY ERASE PREPARE	O	O	F3h					D
PO	SECURITY ERASE UNIT	O	O	F4h					D
ND	SECURITY FREEZE	O	O	F5h					D
PO	SECURITY SET PASSWORD	O	O	F1h					D
PO	SECURITY UNLOCK	O	O	F2h					D
ND	SEEK	M	N	70h			y	y	y
P	SERVICE	O	O	A2h		y	y	y	D
ND	SET FEATURES	M	M	EFh	y				D
ND	SET MAX ADDRESS	O	O	F9h		y	y	y	y
ND	SET MULTIPLE MODE	M	N	C6h		y			D
ND	SLEEP	M	M	E6h					D
ND	SMART DISABLE OPERATIONS	O	N	B0h	y			y	D
ND	SMART ENABLE/DISABLE AUTOSAVE	O	N	B0h	y	y		y	D
ND	SMART ENABLE OPERATIONS	O	N	B0h	y			y	D
ND	SMART EXECUTE OFF_LINE	O	N	B0h	y			y	D
PI	SMART READ DATA	O	N	B0h	y			y	D
PI	SMART READ LOG SECTOR	O	N	B0h	y	y	y	y	D
ND	SMART RETURN STATUS	O	N	B0h	y			y	D
PO	SMART WRITE LOG SECTOR	O	N	B0h	y	y	y	y	D

(continued)