REGISTER ACCESS

The AD7739 is configurable through a series of registers. Some of them configure and control general AD7739 features, while others are specific to each channel. The register data widths vary from 8 bits to 24 bits. All registers are accessed through the communications register, i.e., any communication to the AD7739 must start with a write to the communications register specifying which register will be subsequently read or written.

COMMUNICATIONS REGISTER

8 Bits, Write-Only Register, Address 0x00

All communications to the part must start with a write operation to the communications register. The data written to

the communications register determines whether the subsequent operation will be a read or write and to which register this operation will be directed. The digital interface defaults to expect a write operation to the communications register after power-on, after reset, or after the subsequent read or write operation to the selected register is complete. If the interface sequence is lost, the part can be reset by writing at least 32 serial clock cycles with DIN high and $\overline{CS}$ low. (Note that all of the parts, including the modulator, filter, interface, and all registers are reset in this case.) Remember to keep DIN low while reading 32 bits or more either in continuous read mode or with the DUMP bit and 24/16 bit in the mode register set.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	0	R/$\overline{W}$	6-Bit Register Address					

Bit	Mnemonic	Description
7	0	This bit must be 0 for proper operation.
6	R/$\overline{W}$	A 0 in this bit indicates that the next operation will be a write to a specified register. A 1 in this bit indicates that the next operation will be a read from a specified register.
5–0	Address	These bits specify to which register the read or write operation will be directed. For channel specific registers, the three LSBs, i.e., Bit2, Bit 1, and Bit 0, specify the channel number. When the subsequent operation writes to the mode register, the three LSBs specify the channel selected for the operation determined by the mode register value. The analog inputs configuration depends on the COM1 and COM0 bits in the channel setup register.

Bit 2	Bit 1	Bit 0	Channel	Single Input	Differential Input
0	0	0	0	AIN0–AINCOM	AIN0–AIN1
0	0	1	1	AIN1–AINCOM	AIN2–AIN3
0	1	0	2	AIN2–AINCOM	AIN4–AIN5
0	1	1	3	AIN3–AINCOM	AIN6–AIN7
1	0	0	4	AIN4–AINCOM	AIN0–AIN1
1	0	1	5	AIN5–AINCOM	AIN2–AIN3
1	1	0	6	AIN6–AINCOM	AIN4–AIN5
1	1	1	7	AIN7–AINCOM	AIN6–AIN7

AD7739

I/O PORT REGISTER

8 Bits, Read/Write Register, Address 0x01, Default Value 0x30 + Digital Input Value × 0x40

The bits in this register are used to configure and access the digital I/O port on the AD7739.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	P0	P1	P0 DIR	P1 DIR	RDYFN	REDPWR	0	SYNC
Default	P0 Pin	P1 Pin	1	1	0	0	0	0

Bit	Mnemonic	Description
7, 6	P0, P1	When the P0 and P1 pins are configured as outputs, the P0 and P1 bits determine the pins' output level. When the P0 and P1 pins are configured as inputs, the P0 and P1 bits reflect the current input level on the pins.
5, 4	P0 DIR, P1 DIR	These bits determine whether the P0 and P1 pins are configured as inputs or outputs. When set to 1, the corresponding pin will be an input; when reset to 0, the corresponding pin will be an output.
3	RDYFN	This bit is used to control the function of the $\overline{RDY}$ pin on the AD7739. When this bit is reset to 0, the $\overline{RDY}$ pin goes low when any channel has unread data. When this bit is set to 1, the $\overline{RDY}$ pin will go low only if all enabled channels have unread data.
2	REDPWR	Reduced Power. If this bit is set to 1, the AD7739 works in the reduced power mode. The maximum MCLK frequency is limited to 4 MHz in the reduced power mode.
1	0	This bit must be 0 for proper operation.
0	SYNC	This bit enables the $\overline{SYNC}$ pin function. By default, this bit is 0 and $\overline{SYNC}$/P1 can be used as a digital I/O pin. When the SYNC bit is set to 1, the $\overline{SYNC}$ pin can be used to synchronize the AD7739 modulator and digital filter with other devices in the system.

REVISION REGISTER

8 Bits, Read-Only Register, Address 0x02, Default Value 0x09 + Chip Revision × 0x10

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	Chip Revision Code				Chip Generic Code			
Default	x	x	x	x	1	0	0	1

Bit	Mnemonic	Description
7–4	Chip Revision Code	4-Bit Factory Chip Revision Code
3–0	Chip Generic Code	On the AD7739, these bits will read back as 0x09.

TEST REGISTER

24 Bits, Read/Write Register, Address 0x03

This register is used for testing the part in the manufacturing process. The user must not change the default configuration of this register.

ADC STATUS REGISTER

8 Bits, Read-Only Register, Address 0x04, Default Value 0x00

In conversion modes, the register bits reflect the individual channel status. When a conversion is complete, the corresponding channel data register is updated and the corresponding RDY bit is set to 1. When the channel data register is read, the corresponding bit is reset to 0. The bit is reset to 0 also when no read operation has taken place and the result of the next conversion is being updated to the channel data register. Writing to the mode register resets all the bits to 0.

In calibration modes, all the register bits are reset to 0 while a calibration is in progress; all the register bits are set to 1 when the calibration is complete.

The $\overline{RDY}$ pin output is related to the content of the ADC status register as defined by the RDYFN bit in the I/O port register. The RDY0 bit corresponds to Channel 0, the RDY1 bit corresponds to Channel 1, and so on.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
Default	0	0	0	0	0	0	0	0

CHECKSUM REGISTER

16 Bits, Read/Write Register, Address 0x05

This register is described in the *Using the AD7732/AD7734/AD7738/AD7739 Checksum Register* application note ([www.analog.com/UploadedFiles/Application_Notes/71751876 AN626_0.pdf](www.analog.com/UploadedFiles/Application_Notes/71751876AN626_0.pdf)).

ADC ZERO-SCALE CALIBRATION REGISTER

24 Bits, Read/Write Register, Address 0x06, Default Value 0x80 0000

This register holds the ADC zero-scale calibration coefficient. The value in this register is used in conjunction with the value in the ADC full-scale calibration register and the corresponding channel zero-scale and channel full-scale calibration registers to scale digitally the conversion results of all channels. The value in this register is updated automatically following the execution of an ADC zero-scale self-calibration. Writing this register is possible in the idle mode only (see the Calibration section for details).

ADC FULL-SCALE CALIBRATION REGISTER

24 Bits, Read/Write Register, Address 0x07, Default Value 0x80 0000

This register holds the ADC full-scale calibration coefficient. The value in this register is used in conjunction with the value in the ADC zero-scale and the corresponding channel zero-scale and channel full-scale calibration registers to scale digitally the conversion results of all channels. The value in this register is updated automatically following the execution of an ADC full-scale self-calibration. Writing this register is possible in the idle mode only. The ADC full-scale self-calibration should be used only on +2.5 V and ±2.5 V input voltage ranges (see the Calibration section for details).

CHANNEL DATA REGISTERS

16 Bit/24 Bit, Read-Only Registers, Address 0x08–0x0F, Default Width 16 Bits, Default Value 0x8000

These registers contain the most up-to-date conversion results corresponding to each analog input channel. The 16-bit or 24-bit data width can be configured by setting the 24/16 bit in the mode register. The relevant RDY bit in the channel status register goes high when the result is updated. The RDY bit will return low once the data register reading has begun. The $\overline{RDY}$ pin can be configured to indicate when any channel has unread data or waits until all enabled channels have unread data. If any channel data register read operation is in progress when a new result is updated, no update of the data register will occur. This avoids having corrupted data. Reading the status registers can be associated with reading the data registers in the dump mode. Reading the status registers is always associated with reading the data registers in the continuous read mode (see the Digital Interface Description section for details).

AD7739

CHANNEL ZERO-SCALE CALIBRATION REGISTERS

24 Bits, Read/Write Registers, Address 0x10–0x17,
Default Value 0x80 0000

These registers hold the particular channel zero-scale calibration coefficients. The value in these registers is used in conjunction with the value in the corresponding channel full-scale calibration register, the ADC zero-scale calibration register, and the ADC full-scale calibration register to digitally scale the particular channel conversion results. The value in this register is updated automatically following the execution of a channel zero-scale system calibration.

The format of the channel zero-scale calibration register is a sign bit and a 22-bit unsigned value. Writing this register is possible in the idle mode only (see the Calibration section for details).

CHANNEL FULL-SCALE CALIBRATION REGISTERS

24 Bits, Read/Write Registers, Address 0x18–0x1F,
Default Value 0x20 0000

These registers hold the particular channel full-scale calibration coefficients. The value in these registers is used in conjunction with the value in the corresponding channel zero-scale calibration register, the ADC zero-scale calibration register, and the ADC full-scale calibration register to digitally scale the particular channel conversion results. The value in this register is updated automatically following the execution of a channel full-scale system calibration. Writing this register is possible in the idle mode only (see the Calibration section for details).

CHANNEL STATUS REGISTERS

8 Bits, Read-Only Registers, Address 0x20–0x27, Default Value 0x20 × Channel Number

These registers contain individual channel status information and some general AD7739 status information. Reading the status registers can be associated with reading the data registers in the dump mode. Reading the status registers is always associated with reading the data registers in the continuous read mode (see the Digital Interface Description section for details).

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CH2	CH1	CH0	0/P0	RDY/P1	NOREF	SIGN	OVR
Default	Channel Number			0	0	0	0	0

Bit	Mnemonic	Description
7–5	CH2–CH0	These bits reflect the channel number. This can be used for current channel identification and easier operation of the dump mode and continuous read mode.
4	0/P0	When the status option bit of the corresponding channel setup register is reset to 0, this bit is read as a 0. When the status option bit is set to 1, this bit reflects the state of the P0 pin, whether it is configured as an input or an output.
3	RDY/P1	When the status option bit of the corresponding channel setup register is reset to 0, this bit reflects the selected channel RDY bit in the ADC status register. When the status option bit is set to 1, this bit reflects the state of the P1 pin, whether it is configured as an input or an output.
2	NOREF	This bit indicates the reference input status. If the voltage between the REFIN(+) and REFIN(−) pins is less than NOREF, the trigger voltage, and a conversion is executed, then the NOREF bit goes to 1.
1	SIGN	This bit reflects the voltage polarity at the analog input. It will be 0 for a positive voltage and 1 for a negative voltage.
0	OVR	This bit reflects either the overrange or the underrange on the analog input. The bit is set to 1 when the analog input voltage goes over or under the nominal voltage range (see the Analog Input's Extended Voltage Range section).

CHANNEL SETUP REGISTERS

8 Bits, Read/Write Registers, Address 0x28–0x2F, Default Value 0x00

These registers are used to configure the selected channel, to configure its input voltage range, and to set up the corresponding channel status register.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	BUFOFF	COM1	COM0	Stat OPT	ENABLE	RNG2	RNG1	RNG0
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
7	BUFOFF	Buffer Off. If reset to 0, then the internal buffer is enabled. Operation only with the internal buffer enabled is recommended.
6–5	COM1, COM0	Analog inputs configuration:
4	Stat OPT	Status Option. When this bit is set to 1, the P0 and P1 bits in the channel status register will reflect the state of the P0 and P1 pins. When this bit is reset to 0, the RDY bit in the channel status register will reflect the channel corresponding to the RDY bit in the ADC status register.
3	ENABLE	Channel Enable. Set this bit to 1 to enable the channel in the continuous conversion mode. A single conversion will take place regardless of this bit's value.
2–0	RNG2–RNG0	This is the channel input voltage range:

Analog inputs configuration (Bits 6–5):

Channel	COM1	COM0	COM1	COM0
	0	0	1	1
0	AIN0–AINCOM		AIN0–AIN1	
1	AIN1–AINCOM		AIN2–AIN3	
2	AIN2–AINCOM		AIN4–AIN5	
3	AIN3–AINCOM		AIN6–AIN7	
4	AIN4–AINCOM		AIN0–AIN1	
5	AIN5–AINCOM		AIN2–AIN3	
6	AIN6–AINCOM		AIN4–AIN5	
7	AIN7–AINCOM		AIN6–AIN7	

Channel input voltage range (Bits 2–0):

RNG2	RNG1	RNG0	Nominal Input Voltage Range
1	0	0	±2.5 V
1	0	1	+2.5 V
0	0	0	±1.25 V
0	0	1	+1.25 V
0	1	0	±0.625 V
0	1	1	+0.625 V

CHANNEL CONVERSION TIME REGISTERS

8 Bits, Read/Write Registers, Address 0x30–0x37h, Default Value 0x91

The conversion time registers enable or disable chopping and configure the digital filter for a particular channel. This register value affects the conversion time, frequency response, and noise performance of the ADC.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CHOP	FW (7-Bit Filter Word)						
Default	1	0x11						

Bit	Mnemonic	Description
7	CHOP	Chopping Enable Bit. Set to 1 to apply chopping mode for a particular channel.
6–0	FW	CHOP = 1, single conversion or continuous conversion with one channel enabled. Conversion Time (μs) = (FW × 128 + 262)/MCLK Frequency (MHz), the FW range is 2 to 127. CHOP = 1, continuous conversion with two or more channels enabled. Conversion Time (μs) = (FW × 128 + 263)/MCLK Frequency (MHz), the FW range is 2 to 127. CHOP = 0, single conversion or continuous conversion with one channel enabled. Conversion Time (μs) = (FW × 64 + 213)/MCLK Frequency (MHz), the FW range is 3 to 127. CHOP = 0, continuous conversion with two or more channels enabled. Conversion Time (μs) = (FW × 64 + 214)/MCLK Frequency (MHz), the FW range is 3 to 127.

MODE REGISTER

8 Bits, Read/Write Register, Address 0x38–0x3F, Default Value 0x00

The mode register configures the part and determines its operating mode. Writing to the mode register clears the ADC status register, sets the $\overline{RDY}$ pin to a logic high level, exits all current operations, and starts the mode specified by the mode bits.

The AD7739 contains only one mode register. The two LSBs of the address are used for writing to the mode register to specify the channel selected for the operation determined by the MD2 to MD0 bits. Only the address 0x38 must be used for reading from the mode register.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	MD2	MD1	MD0	CLKDIS	DUMP	Cont RD	24/16 BIT	CLAMP
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
7–5	MD2–MD0	Mode Bits. These three bits determine the AD7739 operation mode. Writing a new value to the mode bits will exit the part from the mode in which it has been operating and place it in the newly requested mode immediately. The function of the mode bits is described in more detail below.

MD2	MD1	MD0	Mode	Address Used for Mode Register Write Specifies:
0	0	0	Idle	
0	0	1	Continuous Conversion	First Channel to Start Converting
0	1	0	Single Conversion	Channel to Convert
0	1	1	Power-Down (Standby)	
1	0	0	ADC Zero-Scale Self-Calibration	Conversion Time for Calibration
1	0	1	ADC Full-Scale Self-Calibration (for 2.5 V)	Conversion Time for Calibration
1	1	0	Channel Zero-Scale System Calibration	Channel to Calibrate
1	1	1	Channel Full-Scale System Calibration	Channel to Calibrate

Bit	Mnemonic	Description
4	CLKDIS	Master Clock Output Disable. When this bit is set to 1, the master clock is disabled from appearing at the MCLKOUT pin and the MCLKOUT pin is in a high impedance state. This allows turning off the MCLKOUT as a power saving feature. When using an external clock on MCLKIN, the AD7739 continues to have internal clocks and will convert normally regardless of the CLKDIS bit state. When using a crystal oscillator or ceramic resonator across the MCLKIN and MCLKOUT pins, the AD7739 clock is stopped and no conversions can take place when the CLKDIS bit is active. The AD7739 digital interface can still be accessed using the SCLK pin.
3	DUMP	Dump Mode. When this bit is reset to 0, the channel status register and channel data register will be addressed and read separately. When the DUMP bit is set to 1, the channel status register will be followed immediately by a read of the channel data register regardless of whether the status or data register has been addressed through the communications register. The continuous read mode will always be dump mode reading the channel status and channel data registers, regardless of the DUMP bit value (see the Digital Interface Description section for details).
2	Cont RD	When this bit is set to 1, the AD7739 will operate in the continuous read mode (see the Digital Interface Description section for details).
1	24/16 BIT	Channel Data Register Data Width Selection Bit. When set to 1, the channel data registers will be 24 bits wide. When set to 0, the channel data registers will be 16 bits wide.
0	CLAMP	This bit determines the channel data register's value when the analog input voltage is outside the nominal input voltage range. When the CLAMP bit is set to 1, the channel data register will be digitally clamped to either all 0s or all 1s when the analog input voltage goes outside the nominal input voltage range. When the CLAMP bit is reset to 0, the data registers reflect the analog input voltage even outside the nominal voltage range (see the Analog Input's Extended Voltage Range section).

MD2	MD1	MD0	Operating Mode	Description
0	0	0	Idle	The default mode after power-on or reset. The AD7739 automatically returns to this mode after any calibration or after a single conversion.
0	0	1	Continuous Conversion	The AD7739 performs a conversion on the specified channel. After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, and the AD7739 continues converting on the next enabled channel. The part will cycle through all enabled channels until it is put into another mode or reset. The cycle period will be the sum of all enabled channels' conversion times, set by the corresponding channel conversion time registers.
0	1	0	Single Conversion	The AD7739 performs a conversion on the specified channel. After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7739 returns to idle mode. Requesting a single conversion ignores the channel setup register enable bits; a conversion will be performed even if that channel is disabled.
0	1	1	Power-Down (Standby)	The ADC and the analog front end (internal buffer) go into the power-down mode. The AD7739 digital interface can still be accessed. The CLKDIS bit works separately, and the MCLKOUT mode is not affected by the power-down (standby) mode.
1	0	0	ADC Zero-Scale Self-Calibration	A zero-scale self-calibration is performed on internally shorted ADC inputs. After the calibration is complete, the contents of the ADC zero-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7739 returns to idle mode.
1	0	1	ADC Full-Scale Self-Calibration	A full-scale self-calibration is performed on an internally generated full-scale signal. After the calibration is complete, the contents of the ADC full-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7739 returns to idle mode.
1	1	0	Channel Zero-Scale System Calibration	A zero-scale system calibration is performed on the selected channel. An external system zero-scale voltage should be provided at the AD7739 analog input and this voltage should remain stable for the duration of the calibration. After the calibration is complete, the contents of the corresponding channel zero-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7739 returns to idle mode.
1	1	1	Channel Full-Scale System Calibration	A full-scale system calibration is performed on the selected channel. An external system full-scale voltage should be provided at the AD7739 analog input and this voltage should remain stable for the duration of the calibration. After the calibration is complete, the contents of the corresponding channel full-scale calibration register are updated, all RDY bits in the ADC status register are set, the $\overline{RDY}$ pin goes low, the MD2–MD0 bits are reset, and the AD7739 returns to idle mode.

RESET

The AD7739 can be reset by the $\overline{RESET}$ pin or by writing a reset sequence to the AD7739 serial interface. The reset sequence is $N \times 0 + 32 \times 1$, which could be the data sequence 0x00 + 0xFF + 0xFF + 0xFF + 0xFF in a byte-oriented interface.

The AD7739 also features a power-on reset with a trip point of 2 V and goes to the defined default state after power-on.

It is the system designer's responsibility to prevent an unwanted write operation to the AD7739. The unwanted write operation could happen when a spurious clock appears on the SCLK while the $\overline{CS}$ pin is low. Note that if the AD7739 interface signals are floating or undefined at system power-on, the part can be inadvertently configured into an unknown state. This could be easily overcome by initiating either a hardware reset event or a 32 ones reset sequence as the first step in the system configuration.

ACCESS THE AD7739 REGISTERS

All communications to the part start with a write operation to the communications register followed by either reading or writing the addressed register. In a simultaneous read-write interface (such as SPI), write 0 to the AD7739 while reading data.

Figure 16 shows the AD7739 interface read sequence for the ADC status register.

SINGLE CONVERSION AND READING DATA

When the mode register is being written, the ADC status byte is cleared and the $\overline{RDY}$ pin goes high, regardless of its previous state. When the single conversion command is written to the mode register, the ADC starts the conversion on the channel selected by the address of the mode register. After the conversion is completed, the data register is updated, the mode register is changed to idle mode, the relevant RDY bit is set, and the $\overline{RDY}$ pin goes low. The RDY bit is reset and the $\overline{RDY}$ pin returns high when the relevant channel data register is being read.

Figure 17 shows the digital interface signals executing a single conversion on Channel 0, waiting for the $\overline{RDY}$ pin to go low, and reading the Channel 0 data register.

DUMP MODE

When the DUMP bit in the mode register is set to 1, the channel status register will be read immediately by a read of the channel data register, regardless of whether the status or the data register has been addressed through the communications register. The DIN pin should not be high while reading 24-bit data in dump mode; otherwise, the AD7739 will be reset.

Figure 18 shows the digital interface signals executing a single conversion on Channel 0, waiting for the $\overline{RDY}$ pin to go low, and reading the Channel 0 status register and data register in the dump mode.
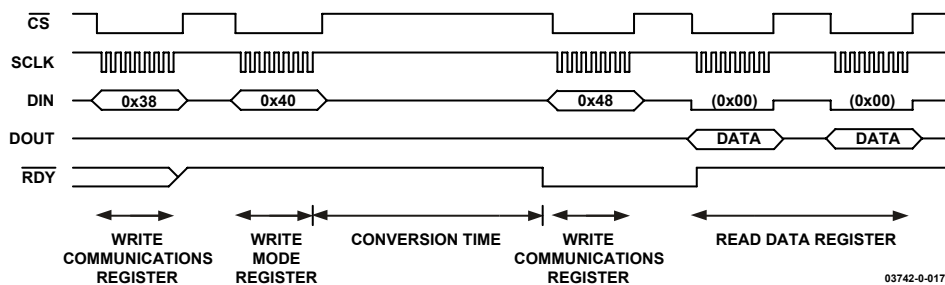

Figure 17. Serial Interface Signals—Single Conversion Command and 16-Bit Data Reading
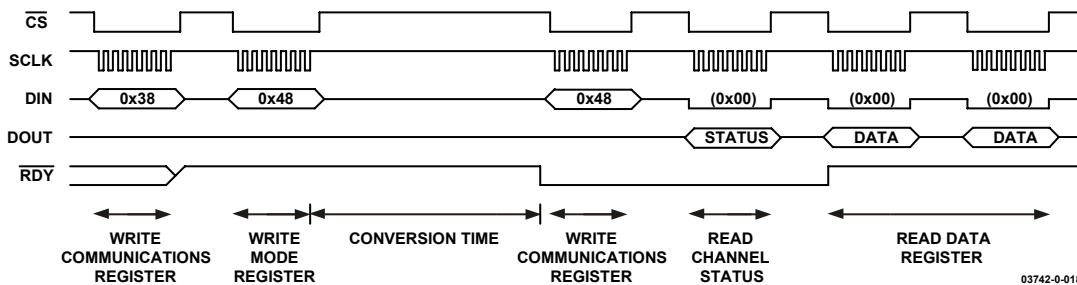

Figure 18. Serial Interface Signals—Single Conversion Command, 16-Bit Data Reading, Dump Mode

CONTINUOUS CONVERSION MODE

When the mode register is being written, the ADC status byte is cleared and the $\overline{\text{RDY}}$ pin goes high, regardless of its previous state. When the continuous conversion command is written to the mode register, the ADC starts conversion on the channel selected by the address of the mode register.

After the conversion is complete, the relevant channel data register and channel status register are updated, the relevant RDY bit in the ADC status register is set, and the AD7739 continues converting on the next enabled channel. The part will cycle through all enabled channels until put into another mode or reset. The cycle period will be the sum of all enabled channels' conversion times, set by the corresponding channel conversion time registers.

The RDY bit is reset when the relevant channel data register is being read. The behavior of the $\overline{\text{RDY}}$ pin depends on the RDYFN bit in the I/O port register. When the RDYFN bit is 0, the $\overline{\text{RDY}}$ pin goes low when any channel has unread data. When the RDYFN bit is set to 1, the $\overline{\text{RDY}}$ pin will go low only if all enabled channels have unread data.

If an ADC conversion result has not been read before a new ADC conversion is completed, the new result will overwrite the previous one. The relevant RDY bit goes low and the $\overline{\text{RDY}}$ pin goes high for at least 163 MCLK cycles (~26.5 µs), indicating when the data register is updated, and the previous conversion data is lost.

If the data register is being read as an ADC conversion completes, the data register will not be updated with the new result (to avoid data corruption) and the new conversion data is lost.

Figure 19 shows the digital interface signal's sequence for the continuous conversion mode with Channels 0 and 1 enabled and the RDYFN bit set to 0. The $\overline{\text{RDY}}$ pin goes low and the data register is read after each conversion. Figure 20 shows a similar sequence but with the RDYFN bit set to 1. The $\overline{\text{RDY}}$ pin goes low and all data registers are read after all conversions are completed. Figure 21 shows the $\overline{\text{RDY}}$ pin when no data is read from the AD7739.
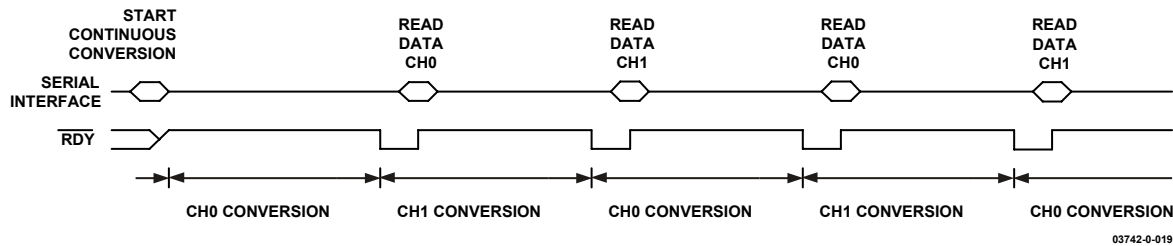

Figure 19. Continuous Conversion, CH0 and CH1, RDYFN = 0
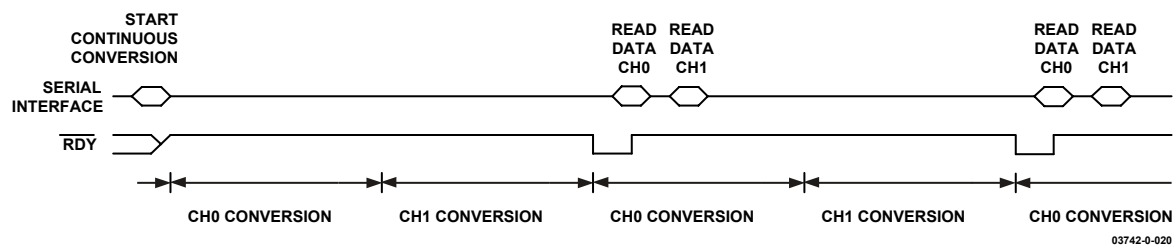

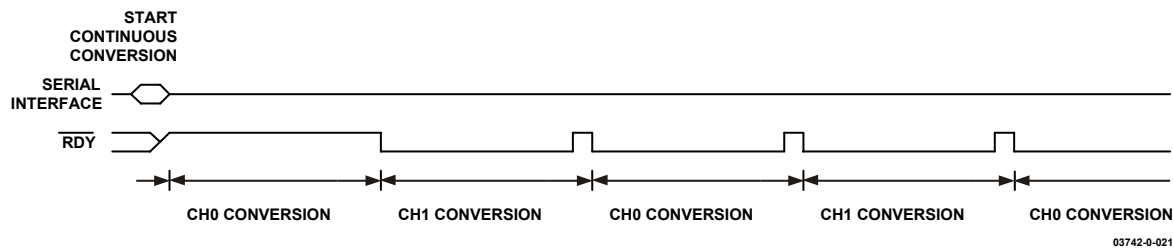Figure 20. Continuous Conversion, CH0 and CH1, RDYFN = 1

Figure 21. Continuous Conversion, CH0 and CH1, No Data Read

CONTINUOUS READ (CONTINUOUS CONVERSION) MODE

When the Cont RD bit in the mode register is set, the first write of 0x48 to the communications register starts the continuous read mode. As shown in Figure 22, subsequent accesses to the part sequentially read the channel status and data registers of the last completed conversion without any further configuration of the communications register being required.

Note that the continuous conversion bit in the mode register should be set when entering the continuous read mode.

Note that the continuous read mode is a dump mode reading of the channel status and data registers regardless of the dump bit value. Use the channel bits in the channel status register to check/recognize which channel data is actually being shifted out.

Note that the last completed conversion result is being read. Therefore, the RDYFN bit in the I/O port register should be 0, and reading the result should always start before the next conversion is completed.

The AD7739 will stay in continuous read mode as long as the DIN pin is low while the $\overline{CS}$ pin is low; therefore, write 0 to the AD7739 while reading in continuous read mode. To exit continuous read mode, take the DIN pin high for at least 100 ns after a read is complete. (Write 0x80 to the AD7739 to exit continuous reading.)

Taking the DIN pin high does not change the Cont RD bit in the mode register. Therefore, the next write of 0x48 starts the continuous read mode again. To completely stop the continuous read mode, write to the mode register to clear the Cont RD bit.
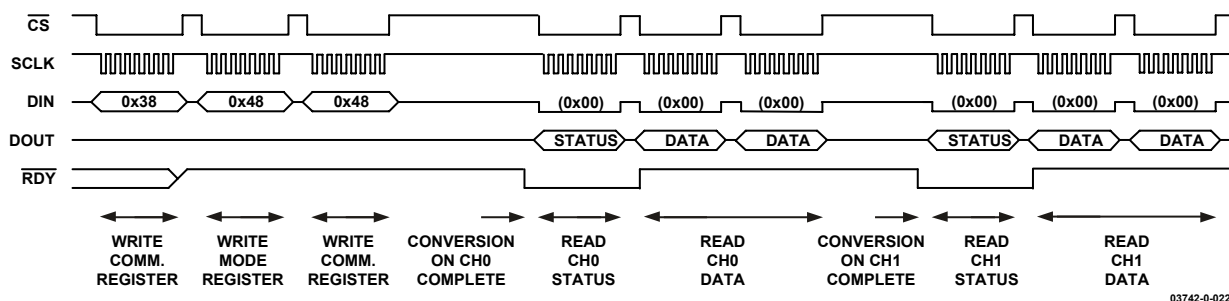

Figure 22. Continuous Conversion, CH0 and CH1, Continuous Read