The UNSW/NICTA FPGA-based GPS Receiver: A Tool for GNSS Research

A G Dempster[1], K Parkinson[1], F Engel[2], P Mumford[1], C Rizos[1], G Heiser[2]

[1]School of Surveying and Spatial Information Systems, University of New South Wales, Sydney, 2052, Australia

[2] National ICT Australia (NICTA), Sydney Node, UNSW, Sydney 2052

Email for corresponding author: a.dempster@unsw.edu.au,

Abstract – The new FPGA-based GPS receiver under development as a joint project by UNSW and NICTA is described. The particular advantages of an FPGA receiver are highlighted, especially those that are consistent with the future research goals of the participants: signal processing algorithms, integration with other sensors and reconfigurability.

1. INTRODUCTION: GNSS: An Exciting Decade Ahead

For a long time, civilians have had easy access to only one Global Navigation Satellite System (GNSS) signal – the GPS L1 signal (carrier 1575.42MHz, chipping rate 1.023Mcps) [1]. To some extent, this has been because researchers and manufacturers have ignored the USSR (now Russian) Glonass system (A notable exception is Topcon, who claim significantly improved performance in their survey receivers that use both GPS and Glonass [2].). The Glonass spectrum is different – a single code frequency 0.511Mcps spreads a series of carriers at 1602.0+0.5625n MHz, n = 1..12 [3].

In the next few years, there will be a large number of new GNSS signals available. Soon GPS will provide a second civilian signal on L2 (carrier 1227.6 MHz) [1, 4] and a new signal on L5 (carrier 1176.45 MHz, chipping rate 10.23Mcps) [5, 6, 7]. The European Galileo system will have several signals available to commercial users. Open services (OS) are available on E5 (1164-1215MHz) and E2-L1-E1, known for convenience as L1 (1559-1592Mz). Commercial services (CS), for which a fee is required but are not restricted to security services, are available on E6 (1215-1300MHz) and L1. At the time of writing, the above frequency allocations were the latest to have been formally released [8, 9], although it is known that they will change because of agreements between the Galileo and GPS teams [10, 11]. The OS L1 signal bandwidth, for instance, has been reduced by a factor of 2 so that it has a 1.023MHz chipping rate, and a binary offset code of 1.023MHz, a so-called BOC(1,1) code.

The locations of the GNSS signals in the spectrum are indicated in Figure 1.

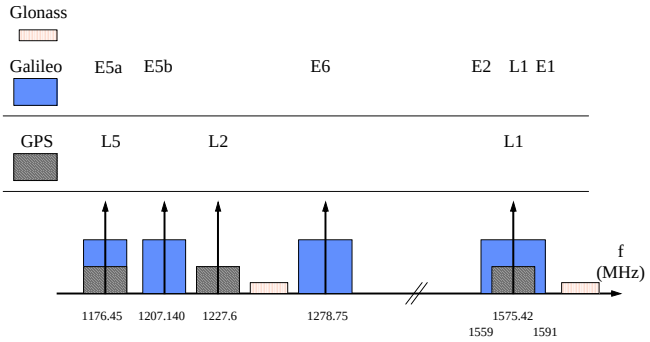

Figure 1. Spectral Locations of GNSS Signals

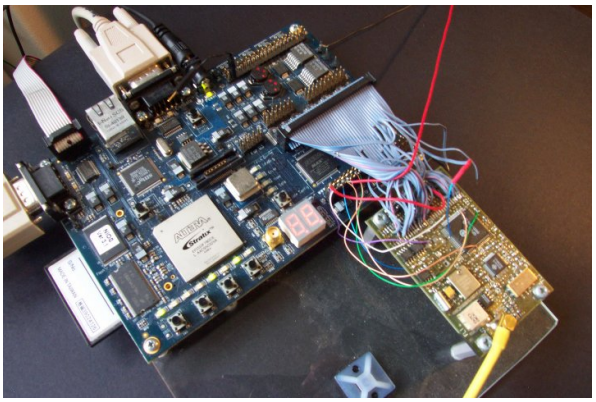

Figure 2 Modified Canadian Marconi SuperStar board interfaced to Altera Stratix development system.

In addition to the stand-alone GNSS, there are also a number of augmentation systems that will be transmitting in the Navigation bands. The EGNOS, WAAS and MSAS systems transmit "GPS-like" compatible signals at the L1 carrier frequency (e.g. see [12]) that increase the integrity of the GPS system, i.e. they allow rapid reporting and elimination of rogue satellite measurements. These signals have been available for some time. New augmentation signals are currently being defined, however, for the Japanese QZSS [13] and the Indian GAGAN [14].

In total, then, civilians may have 7 new signals (2 GPS, 3 Galileo, QZSS and GAGAN) available in the next decade.

2. FPGA GPS RECEIVER DEVELOPMENT

2.1. Scope of Development

In 2004, UNSW and NICTA launched a development of a new GPS L1 receiver – to be based on an FPGA [15]. The Zarlink GP2015 RF front end would interface directly with the FPGA, which would perform all of the baseband processing and higher-level processor based tasks. In a more typical Zarlink arrangement, that functionality would be performed by a pair of chips, the GP2021 baseband chip and ARM60 processor, or the GP4020 chip, which contains both the processor (an ARM7) and baseband functions.

The aim was also to have a very generic design, which could cope with different, or several, RF front end chips. It would also have a range of interfaces for transporting data out of the receiver: RS232, JTAG, Ethernet and USB-2.

2.2. Approach

The initial approach was as follows:

- Migrate the processor and firmware to the FPGA.
- Migrate the digital baseband functionality to FPGA
- Design a new stand-alone circuit board that has the Zarlink front end.

The implementation of this plan involved taking the circuit board from a Canadian Marconi SuperStar board and gradually migrating functions into the FPGA. The FPGA selected was an Altera Stratix, which was large enough to implement a simple L1 receiver. The hardware for this phase is shown in Figure 2.

3. PROGRESS

At the time of writing, the processor and firmware have been successfully ported in the FPGA and the baseband processing is in process. The first plot of a correlation is shown in Figure 3. It is taken from an off-air signal, from an antenna on the roof of the EE building at UNSW and clearly shows a successful acquisition of a signal in noise using the new correlator.

Figure 4 shows the new stand-alone receiver board. The Zarink RF front end is in the shielded box. For this board, the larger Altera Cyclone FPGA was baselined in order to make it possible to perform more elaborate research functions in addition to the standard baseband processing. Unfortunately, noise simulations predicted that the USB-2 interface would interfere too severely with the RF section so it was omitted. Figure 5 shows the block diagram of the new board

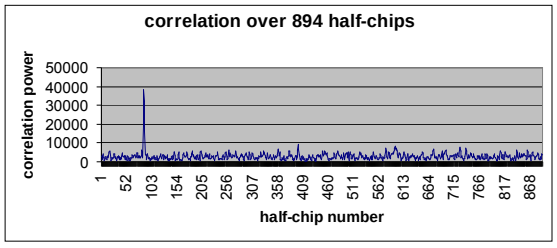

Figure 3 The first correlation from the FPGA receiver

4. USING THE NEW RECEIVER AS A RESEARCH PLATFORM

4.1. New Signal Processing Algorithms

The key component of a GNSS receiver's digital hardware is the "correlator", a generic title given to the hardware that performs the matching of the transmitted CDMA code with the local code generated in the receiver. It de-spreads the spread spectrum signal and allows accurate estimation of the signal's time of arrival. The correlator design dictates the receiver's performance in the presence of multipath (e.g. [16, 17]) and interference [18], and when strong GPS signals interfere with weak ones [19]. The UNSW group is investigating all of these

areas. However, the correlator design in a given chip set is fixed and cannot be modified to test new ideas. Hence a configurable FPGA design is attractive

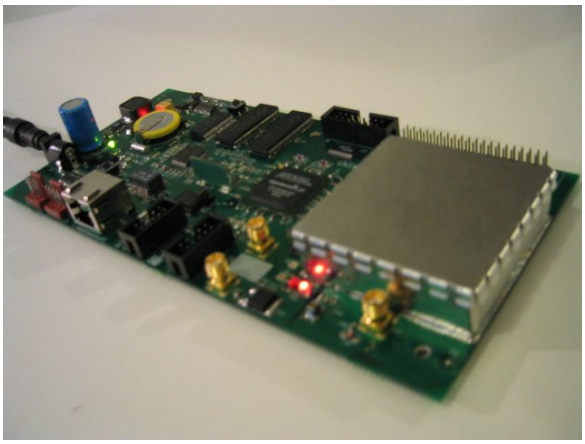

Figure 4 The new FPGA board

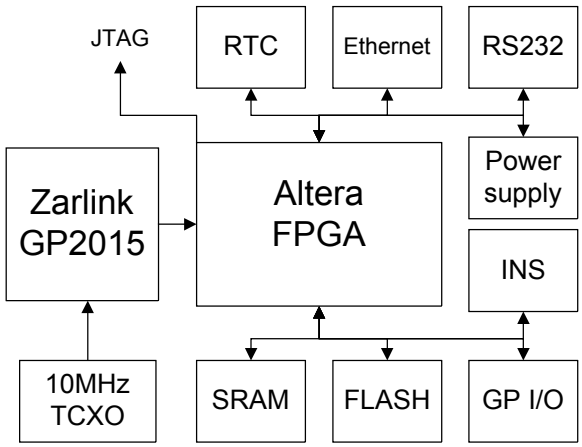

Figure 5 Main functions in the new FPGA receiver

4.2. New Methods of Integration with Other Sensors

Traditional methods of integrating a GPS receiver with an inertial navigations system (INS) use "loose" or "tight" coupling. The first of these methods uses the position from the receiver, and the second uses raw pseudorange measurements. In other words, no modification needs to be made. However, in order to make "ultra-tight" integrations [20], there must be access to the receiver's tracking loops. This is not possible with any commercial chip set, so until a chip set is produced that is designed for use in ultra-tight integrations, the only way to design and test these techniques is with a receiver such as this one. The new version of the GPS receiver board contains a 3 axis accelerometer that is connected to the FPGA to assist in research in this area.

Other techniques designed both to aid tracking and integrate signals from other sensors, such as the "vector delay-locked loop" (VDLL) [21] also require intervention within the loop.

UNSW is researching both of these types of receiver.

4.3. Reconfigurability

Galileo satellites will be gradually launched over the next 10 years, so it will be a long time before the whole constellation is available; however, individual satellites should be visible soon. It seems then to be sensible not to design a receiver with huge numbers of Galileo correlators, because they will mostly lie unused for a long time. To have the capability of using those signals when available would also be desirable, because they are better than existing GPS signals. This is one argument for designing a receiver that could today have its hardware assigned to be L1 GPS, but later evolve so that it uses the best signals visible. An FPGA lends itself to being reconfigured, and this type of reconfigurable hardware would also be useful from other points of view which may not currently be known.

5. DESIGN CHALLENGES

As with most low level CDMA signals, those used for GPS are extremely weak by the time they reach the earth's surface. This presents some technical challenges in most cases when designing a GPS receiver. In particular, there is always some risk when designing receiver circuitry of interference from the adjacent digital electronics. What makes the conditions less ideal in this case is that in the FPGA environment, there is plenty of opportunity to radiate rich harmonics that can compromise the main GPS signals. A particular problem, of course, is that the exact nature of any future FPGA circuit cannot be predicted, so it is difficult always to know the exact nature of this interference. Certain relevant characteristics of the FPGA are programmable, however. Significant effort has been directed towards ensuring the current L1 signals are not interfered with in this receiver platform, and will hopefully be presented at the GNSS 2005 conference in Hong Kong.

6. EXTRACTING THE MEASUREMENTS

Measurement data must be easily extractable using desktop computers. Because GPS data can consist of high speed and high volume measurements, the obvious interface, RS232, may at times be limiting. In this case 100BaseT Ethernet has been provided with the ability to install the Media Access Controller inside the FPGA. Again, the re-configurability of the FPGA allows plenty of flexibility in the communications area.

7. CONCLUSION

There is a strong case for using an FPGA for GPS receiver design because of the ability to easily re-configure the digital processing environment. With many new signals arriving over the next decade this gives the design "future proofing". It also allows many types of research to be carried out. Planned future enhancements to the receiver platform include the addition of different interfaces and the design of multiple RF front end options for the proposed new signal frequencies.

8. REFERENCES

[1] ICD-GPS-200C, "Interface Control Document: Navstar GPS Space Segment/ Navigation User Interfaces", US DOD, IRN-200C-005R1, 14 Jan 2003

[2] Topcon Australia website; http://www.topcon.com.au/gps/GPSGLONASS.htm

[3] "GLONASS Interface Control Document", version 5, 2002, available from http://www.glonass-center.ru/icd02_e.zip (also RTCA Paper No. 639-95/SC 159-685)

[4] R D Fontana et al, "The Modernized L2 Civil Signal", GPS World, Sep 1, 2001

[5] ICD-GPS-705, "Interface Control Document: Navstar GPS Space Segment/ Navigation L5 User Interfaces", US DOD, 29 Mar 2002

[6] RTCA SC-159, "DO-261 Navstar GPS L5 Signal Specification", 14 Dec 2000, $90

[7] A J Van Dierendonck, "The New L5 Civil GPS Signal", GPS World, Sept 2000, pp64-71

[8] Hein et al, "Status of Galileo Frequency and Signal Design", Proc ION-GPS 2002

[9] Hein et al, "Galileo Frequency and Signal Design", GPS World, June 2003, pp30-37

[10] "GPS and Galileo Reach Signal Agreement", Global View, GPS World, Mar 2004, pp12-13

[11] "EC: GPS-Galileo Deal Has Mutual Benfits", Global View, GPS World, Apr 2004, p 13

[12] Federal Aviation Administration Specification Wide Area Augmentation System (WAAS) FAA-E-2892B, 21 Sep 1999, http://www.faa.gov/asd/international/GUIDANCE_MATL/2892b_c1.pdf

[13] Takeshi Ono, Isao Kawano, Satoshi Kogure "Test Bed for Satellite-based Positioning System using Quasi-Zenith-Satellites" Proc GNSS 2004, Sydney, Australia, 6–8 December 2004

[14] A.K. Sisodia, J.K. Hota, N.J. Vora, Asif Siddiqui, H.C. Sanandiya, S.C. Bera, "Indian SBAS GAGAN", Proc ION-GPS/GNSS 2003, Portland Oregon, 10-12 Sept 2003

[15] Frank Engel, Gernot Heiser, Peter Mumford, Kevin Parkinson, Chris Rizos "An Open GNSS Receiver Platform Architecture", Proc GNSS 2004, Sydney, Australia, 6–8 December 2004

[16] van Nee, R.D.J.; The Multipath Estimating Delay Lock Loop, IEEE ISSTA 92. Nov 29-Dec 2, 1992 pp39 - 42

[17] Jason Jones, Pat Fenton, Brian Smith, "Theory and Performance of the Pulse Aperture Correlator", NovAtel Inc., 9 June 2004, http://www.novatel.com/Documents/Papers/PAC.pdf

[18] Asghar Tabatabaei Balaei, Joel Barnes and Andrew G. Dempster, "Characterization Of Interference Effects On Gps Signal Carrier Phase Error" To be published in Proc. SSC 2005 Spatial Intelligence, Innovation and Praxis, The Spatial Science Institute, September, 2005. Melbourne

[19] E P Glennon and A G Dempster, "A review of Cross-Correlation Mitigation Techniques", Proc GNSS-2004, Sydney Dec 6-8 2004

[20] S.Ravindra Babu and Jinling Wang, "Comparative study of interpolation techniques for ultra-tight integration of GPS/INS/PL sensors" Proc GNSS-2004, Sydney Dec 6-8 2004

[21] B W Parkinson and Spilker (eds), Global positioning system :theory and applications,

Washington, DC :American Institute of Aeronautics
and Astronautics,1996.