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FPGA based GPS receiver design considerations

K J Parkinson, A G Dempster, P Mumford, C Rizos
Satellite Navigation and Positioning Group
School of Surveying and Spatial Information Systems
University of New South Wales
Sydney NSW 2052 Australia
E-mail: k.parkinson@student.unsw.edu.au
a.dempster,p.mumford, c.rizos]@unsw.edu.au

Presenter: Andrew Dempster

ABSTRACT

A project to build a GPS receiver using an FPGA for base-band processing began in 2004. The new receiver platform uses a commonly available RF front end ASIC to convert the GPS signals to a suitable IF. The digital design for baseband processing is normally a reasonably straight forward task. However, because the received GPS signals are at such low levels this presents some challenges. One of the main considerations is to avoid contamination of the incoming signals with interference that can be generated from the digital electronics when using an FPGA. In this paper we describe the hardware design process with a focus on avoiding interference while still allowing complex FPGA logic to operate alongside sensitive GPS RF signal processing.

FPGA, GPS Receiver, CDMA.

1. INTRODUCTION

As outlined previously [1], this project to build a GPS receiver using an FPGA for the base-band processing function was started with the aim of providing a general purpose GPS research platform. While the FPGA allows many options for signal processing, it presents some interesting challenges to the overall electronic design.

So far most GPS receiver design information, especially inside the silicon components, has remained proprietary. In recent years there has been an increase in GPS receiver “chip-set” offerings accompanied by vendor reference designs suggesting a least-risk development path. There are often technical risks associated with deviating too far from this reference design. These chip sets allow custom receiver designs to be created and in many cases integrated into new products. Signav has been one of the top end pioneers in this area, licensing a complete hardware and software reference design based on the Zarlink chips[2].

In the normal design process for a GPS receiver, some care is needed to integrate the potentially noisy digital base-band processor with sensitive Radio Frequency (RF) components. The incoming GPS signal is of the order of -160dBW which can easily be disturbed by the radiated harmonics from square waves found in the digital area of the receiver.

Most RF front end chips have some form of matching silicon interface to their partner base-band processing ASIC, leading to less interference problems. In this project one of the challenges was to connect the RF front end to the general purpose FPGA interface while minimising the risk of interference to the GPS signal.

In this paper we focus on the selection of a suitable RF front end chip, the hardware aspects of integrating the selected chip with the FPGA and minimising GPS signal contamination.

2. THE RF FRONT END

Since the launch of GPS in the early 1980's, the advances in RF semiconductor technology have been significant. Most of this has been driven by larger market forces such as mobile telephones and RF Local Area Networks. As these new materials and fabrication methods have been applied to the GPS receiver front end, the availability of improved GPS RF chips has increased. These chips typically contain an RF amplifier followed by mixing of the signal down to an Intermediate Frequency (IF) with filtering to eliminate out-of-band signals. The L1 GPS signal (1575.42MHz) normally arrives at an IF that can be comfortably sampled by a base-band processor. In many cases the signal is digitised into a data stream beforehand. See **Figure. 1.**

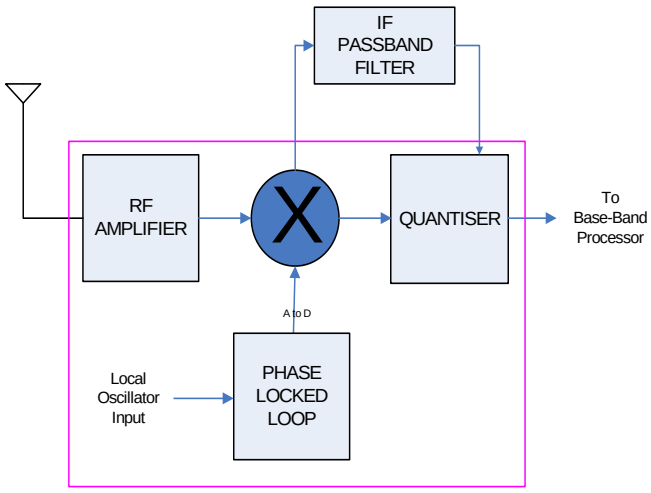

Figure 1. GPS RF Front end architecture

Many of the major silicon vendors now offer receiver RF front end chips that are either specifically designed for GPS, or more general purpose chips that can be adapted to the task. These chips provide good performance with the L1 signal when combined with a suitable Low Noise Amplifier (LNA) as the first stage after the antenna. Detailed design of the internals of a typical front end is given by Shaeffer in [3] and also in [4].

Because of the general increase in both silicon density and speed of Application Specific Integrated Circuits (ASIC) over the past few years, the typical base-band processing ASIC has become much faster and less power hungry. This part normally costs less to produce than the higher density front end chip because it has no analogue functions and uses a common high yield fabrication process.

As a result of this, some GPS chip set designers have been able to use fewer down conversions in the RF front end chips to cut costs and take advantage of the higher speed of the base-band processors. With fewer down conversions, the IF or quantised output from the RF front end arrives at the base-band processor at a much higher frequency. The simplicity of this is attractive where GPS receiver functions are to be integrated into a mass produced consumer product. However, where better GPS receiver performance is required, such as working with carrier phase and high immunity to jamming, a multiple down conversion RF system is more desirable.

A number of front end chips were considered for this project some of which are compared in **Table 1.** This list is by no means exhaustive and only shows some of the likely contenders including the Zarlink GP2015 [5] which was finally chosen.

Table 1.

R	M	R f	N C	O	D
NJ1006A	Nemerix	16.367MHz	2	2 bit sign+mag	On board LNA
GP2015	Zarlink	10MHz	3	2 bit sign+mag	GPS + GLONASS
ATR0600	Atmel	23.104MHz	1	2 bit, 4.35MHz	Low power
UAA1570HL	Philips	14.4MHz	2	1 bit sign+mag	GPS + GLONASS
SE100L	SiGe	16.368MHz	1	1 bit, 4.092MHz	
GRF2i/LP	SiRF	16.368MHz	2	2 bit	
CXA1951AQ	Sony	16.368MHz	2	4.092MHz IF	Low power
STB5610	ST	16.368MHz	2	4.092MHz IF	On board LNA
uN1005	uNav	19.2MHz	Direct	2.031MHz IF	SPI interface

2.1 THE GP2015

The Zarlink GP2015 RF front end chip has been available for some years and is currently used in commercial GPS receiver products from Novatel [6] and Signav [2]. It was first conceived by GEC Plessy as part of their GPS chip set, then became a Mitel Semiconductor product and is now available from Zarlink Semiconductors. Being a triple conversion front end it is not so popular with manufacturers in the mass markets because of the increased complexity of the off chip IF components. However, ignoring cost, triple conversion is an advantage for this project because it helps with interference rejection. The successive IF stages with sharp cut-off and deep stop-band filters allow good rejection of out of band signals. The overall quality of the output signal allows for good GPS code and carrier phase measurements as is found in other receivers that use this chip, i.e. the Novatel Superstar [7]. The Zarlink chip set is well documented with application information gained from a GPS development system promoted by GEC Plessy [8] [9].

2.2 LNA

The latest improvements in semiconductor technology are also seen in the LNA. The main requirement in this area of a receiver is to have the highest gain with the lowest noise. The minimum noise contribution of the LNA is very important in a spread spectrum application like GPS where the signal to be detected is below the noise threshold. Minimising the noise through the LNA and RF front end allows the correlator in the base-band processor a higher signal to noise ratio to work with, leading to more robust signal detection and tracking. **Table 2** is a condensed list comparing some of the LNA chips considered for the GPS front end in this project.

Table 2.

Part	Manufacturer	Noise figure	Gain
MGA-87563	Agilent	1.6dB	14dB
ATR0610	Atmel	1.5dB	15dB
MAAM12021	MACOM	1.55dB	21dB
BGA427	Infineon	2.2dB	18.5dB

The LNA chosen for this project was the Agilent MGA-87563 [10], mainly for its availability and low minimum order quantity. This is a miniature SOT-363 Gallium Arsenide (GaAs) device that was designed for 2.4GHz applications. It has excellent gain of 14dB at 1575MHz with a noise figure of 1.6dB at 25^{o}C. Correct impedance matching of the device is critical to achieving the stated noise figure. Fortunately this is less problematic because the input is partially matched internally to 50 ohms. In this case a simple conjugate matching circuit using a small series inductance of 8.2nH gave good results.

Printed Circuit Board (PCB) layout is critical when designing at this frequency. Adequate grounding is required for maximum performance and stability of the LNA. All ground planes around the part were connected by multiple plated through holes (vias) that have a diameter no smaller than the thickness between the two outermost PCB layers. This minimised the inductance in the ground connections.

Signal paths are designed around strip-line dimensions that maintain the correct impedance for both input and output.

3. FPGA

In a conventional GPS receiver the base-band and microprocessor functions are often combined into one ASIC. This same architecture has been used in this project, the difference being that the FPGA has replaced the ASIC.

The FPGA chosen for this project was an EPM2C35 in a 484 pin BGA package from the Altera Cyclone II family [11]. This device has 33,216 logic elements and 105 memory blocks of 4608 bits.

This FPGA is divided electrically into 2 parts: the cental core and the Input/Output cells. The central core contains all of the programmable logic functions including RAM and operates

from a 1.2 volt supply. The I/O cells provide buffered connections to the off-chip electronics and operate from a 3.3 volt supply.

3.1 Fine tuning the FPGA to minimise interference

One of the features of the FPGA is the ability to re-configure the slew rates of different parts of the logic core and I/O pins. The Altera “programmable output drive strength” option allows reduction of the slew rate of I/O pins. This was used to slow the rise time of most of the I/O signals and reduce interference.

During testing it was also possible to re-route long internal connections that were generating noise by using the floor plan editor to optimise them inside the FPGA after design was compiled and fitted into the device. This is a manual procedure similar to building an ASIC but in this case being able to optimise it further after the chip is on the board was an advantage.

These iterative approaches to locating and reducing noise spikes with a spectrum analyser using this approach gave good results, even though somewhat time consuming. **Figure 2** shows the effect of changing the slew rate.

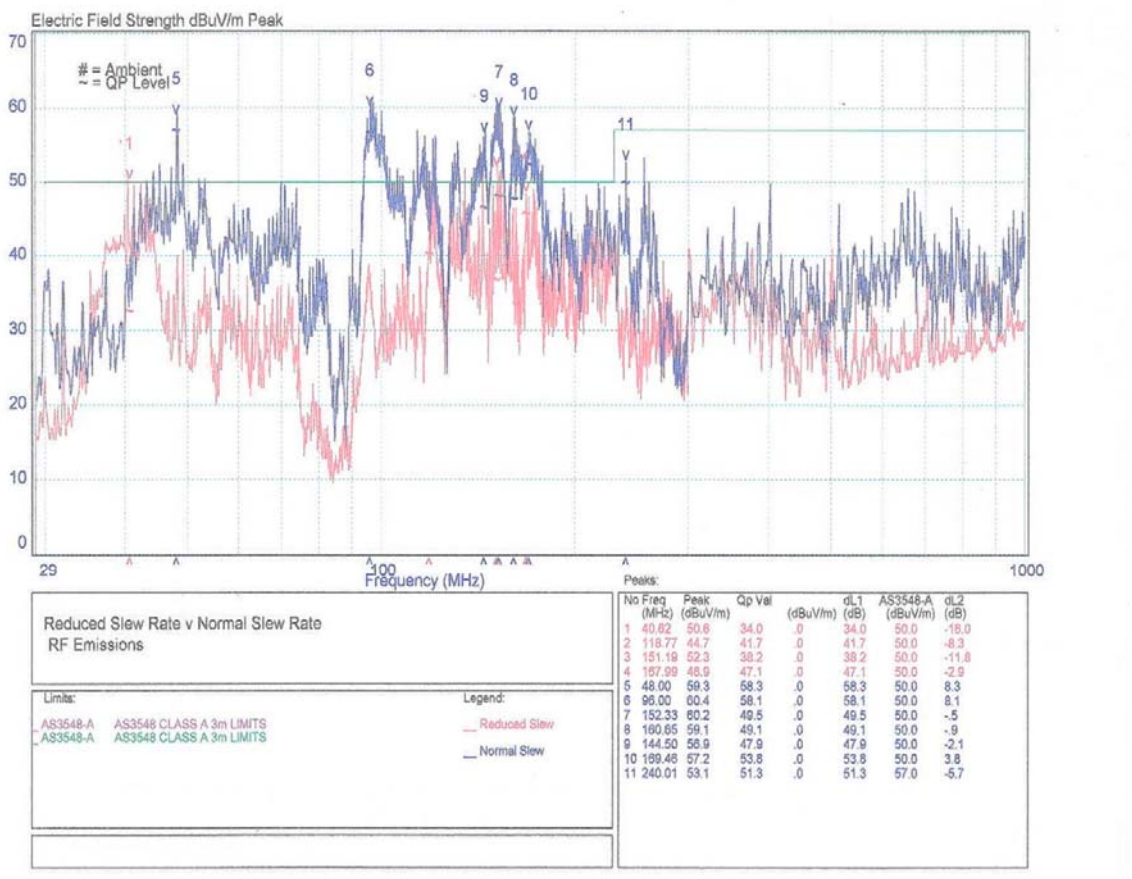

Figure 2 Noise measurements before (blue) and after (red) FPGA tuning, compared to AS3548-A (green).

The blue trace (top) is measured with no attempt to minimise the noise while the red trace is after successive changes to the FPGA. Note that these measurements are compared to the Australian Electro Magnetic Interference (EMI) standard AS3548-A which is considered to be a good baseline for comparing interference measurements.

3.2 Interfacing to the FPGA

The majority of the FPGA connections to the external RAM and other peripheral chips used conventional single-ended CMOS I/O voltage levels.

The main clock signal is supplied by the GP2015 at 40MHz using a Low Voltage Differential Signalling (LVDS) method. As shown by Granberg [12], this form of transmission is less susceptible to common-mode interference than single ended schemes and is ideal for this environment where every effort to reduce harmonic radiation is needed. The FPGA allows most I/O paths to use LVDS, including clock inputs. The down side is that each I/O path needs 2 pins on the FPGA. In this case the GP2015 clock signal is a sine wave, not a square wave as normal, thus further reducing radiated harmonics. This sine wave is fed directly into the on board phase locked loop in the FPGA where it is converted to a square wave internally for use globally by the logic. See **Figure 3.**

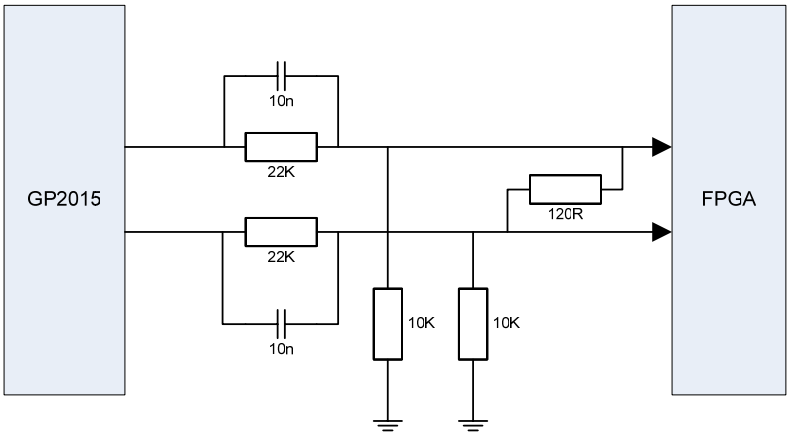

Figure 3. LVDS clock connections to the FPGA

As explained in the ANSI LVDS standard [13] it is important for the terminating resistor to be mounted as close as possible to the receiving device to achieve maximum noise immunity.

4. PC BOARD LAYOUT

The PCB design used 8 layers structured as shown in **Table 3**. A generous copper flood of 0.01” clearance was used around power and ground areas on all layers.

Table 3.

Layer Number	Function
1	Top signal routing layer

2	Ground plane
3	+3.3 volt plane
4	Signal routing layer
5	Signal routing layer
6	Signal routing layer
7	Signal routing layer
8	Bottom signal routing

4.1 Component placement

In general the board is divided into 2 areas: one for the RF components and the other for the rest of the components. As shown in **Figure 4,** the FPGA is located centrally between the RF components on the right and the peripherals on the left. The switch-mode power supply section is located at the extreme left end of the board from the RF section to give maximum isolation.

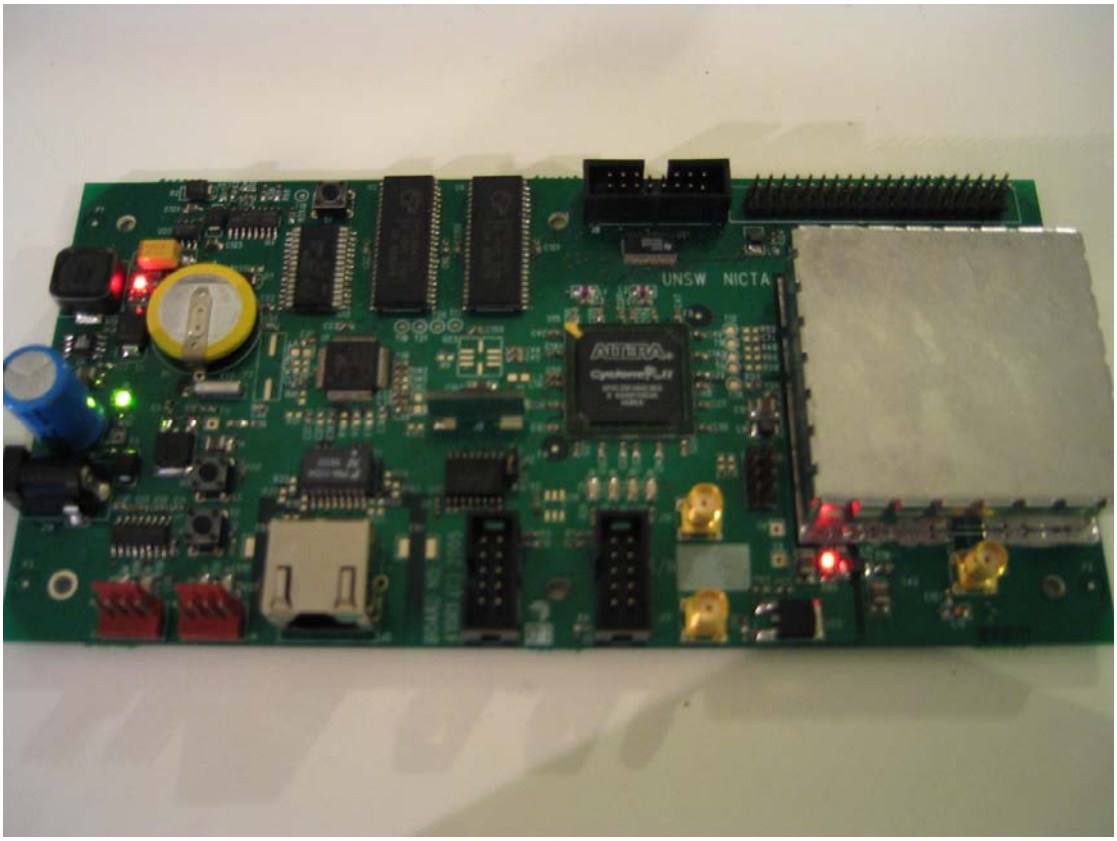

Figure 4 The new FPGA receiver board

4.2 FPGA Grounding

An area of copper flood under the FPGA was used as a power plane to bring the 1.2 volt supply to the core of the device. This provides a low impedance path for the supply and the large number of bypass capacitors required on these pins.

4.3 RF Shield

All RF front end components on the top side of the board, including the LNA and 10MHz oscillator, are housed inside a metal screen to further reduce unwanted interference. This is a common practice in most GPS receiver designs and gives a small improvement, mostly from external interference.

4.4 Bypass capacitors

A new type of multi-layer ceramic capacitor known as “the tantalum replacement” was used for all power supply bypass functions. This part, as described by Murata [14], is constructed as a monolithic block of ceramic containing two sets of interleaved planar electrodes that extend to opposite sides of the dielectric. The result is a very small form factor capacitor with low Equivalent Series Resistance (ESR) and low lead inductance. Furthermore, these devices are far more effective for bypassing unwanted interference signals to ground. None of these parts were available when the GP2015 was conceived and are not included in any reference design recommendations. However, they are used to both then FPGA and the RF section to good effect.

3. CONCLUDING REMARKS

The design presented some difficult challenges because the interfering digital circuitry is expected to perform normally without compromising the sensitive RF circuity. From extensive testing most of the problems have been identified and cured. However, in a future revision of the design there will opportunities to make further improvements where this is not currently physically possible.

While this receiver is designed to work with the L1 GPS signal only, further development work in the RF front end area will allow the reception of L2 and L5 signals. Limitations to the frequency plan of GP2015, in particular the 2MHz bandwidth of the 3rd IF stage, prevent working with some of the new GPS signals that will be available in the near future. This may mean using a different RF front end chip with different filtering line up around the LNA in the future.

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