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Improving signal quality in FPGA based GPS receiver designs

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ABSTRACT

The design of a new FPGA based GPS receiver platform for research purposes is discussed with emphasis on the efforts to reduce low level signal contamination from the nearby digital circuitry. A key objective is to acquire the highest quality low interference GPS signals at the front end to allow signal processing research. The receiver uses a front end ASIC to convert the GPS signals to a suitable IF in the normal way, followed by an FPGA to perform the base-band processing functions. The digital noise generated by the FPGA creates some challenges when operated alongside the RF front end when receiving GPS signals at very low levels. The focus of this paper is on the architecture used and the electronic design methods used to reduce interference.

KEYWORDS: FPGA, GPS Receiver, L1, L2.

1. INTRODUCTION

A GPS receiver using a Field Programmable Gate Array (FPGA) called the Namuru was launched by UNSW and NICTA in 2005 with the aim of being a flexible platform for GPS signal processing research [1]. The FPGA approach is primarily to replace the Application Specific Integrated Circuit (ASIC) which is normally used for the baseband processing function in a typical GPS receiver. The FPGA now replaces both the baseband and CPU functions by combining these both into logic in this receiver design. Because the FPGA is a programmable device, it allows a multitude of signal investigating scenarios to be explored. Furthermore, the ability to use the parallel processing capabilities of pure logic allows some of these schemes to process the same signals in real time for comparative studies. This receiver was created as a very generic design using a single Zarlink GP2015 RF front end [2] to reduce the L1 GPS signal from 1575.42 MHz to an Intermediate Frequency (IF) of 4.309 Mhz. for processing in the FPGA. A range of interfaces are provided to extract measurement data from the receiver: RS232, JTAG, Ethernet and general purpose I/O pins.
Further work has commenced to add extra RF front end components that will allow access to new GPS signals that are becoming available in the near future.

2. THE RF FRONT END

As described [3], the RF front end ASIC typically contains an RF amplifier followed by mixing of the L1 signal (1575.42MHz) down to an Intermediate Frequency (IF) with filtering to eliminate out-of-band signals. The GPS signal finally arrives at an IF that can be easily sampled by a base-band processor, as shown in **Figure 1.**

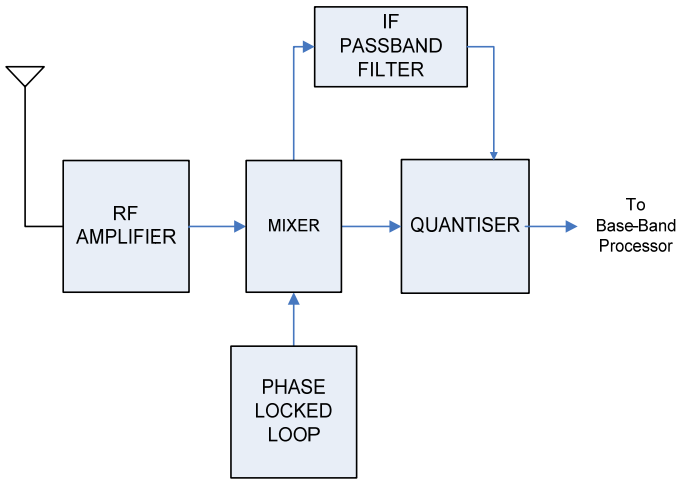

Figure 1. GPS RF Front end architecture

2. MINIMISING UNWANTED NOISE

Because of the extremely low level of the GPS signals (in the order of -160dB), the design tasks associated with even a medium to low performance receiver are somewhat challenging [3]. There is often a risk of signal contamination within the receiver's sensitive components when operated alongside the digital section. The use of an FPGA in the Namuru receiver further increased this problem because of the inherently noisy environment they provide,

more so than an ASIC. In an FPGA the typical design objective is to keep the rise times as short as possible to maintain the setup and hold times around the logic. Naturally, this produces a broad spectrum of harmonic interference which is capable of smudging the incoming GPS signal and producing spectral spurs capable of interfering with the IF performance of the RF front end circuit. These signals, when strong enough, will behave as jamming signals, causing the Automatic Gain Control (AGC) to attenuate the L1 signal to a level where there is risk of loss of satellite signal lock.

The interference can enter the RF section either by being radiated from the FPGA or it can be carried into the area through power supply lines. The main objectives are to reduce the generation of noise at the source and to block this from entering the RF front end as much as possible.

Several approaches were taken in the Namuru receiver to ensure that the problem is kept to a minimum.

2.1 Sheilding

A metal shield was placed around the sensitive RF front end components to create a barrier for radiated noise. Some of the tracks and inductors in the RF circuitry can act as effective antennas which are capable of picking up unwanted signals at similar frequencies. The shield provided the combined effect of reducing both FPGA and outside interference.

2.2 Power filtering

Extensive power supply filtering was employed to decouple any noise generated in the digital circuitry from the RF front end. Two measures were used in particular, to overcome this problem: firstly the RF circuitry is driven from a stand alone linear voltage regulator to provide maximum isolation from the digital switch mode regulator. Secondly, the generous use of low ESR multi-layer ceramic capacitors on the supply rail to bypass any unwanted noise is very effective.

2.3 Printed Circuit Board Layout

PCB layout is critical to overall performance. The PCB is divided into two distinct areas separating the digital area from the RF section. Power and ground planes on internal layers of the PCB provide a low impedance path for supply and bypass capacitors. It is important in the RF section to make sure that no power supply and digital tracks run close to the inductors in sensitive parts of the circuit. A ground flood of copper is used on the top and bottom layers to provide additional shielding around components. However, it is important that this flood is not closer than 0.3mm to avoid capacitive coupling of any unwanted ground based signals running through the copper flood.

2.4 Reducing FPGA I/O slew rate

The Altera Cyclone 2 FPGA (EPM2C35F484) [4] used in the receiver is designed with the ability to control the slew rates of the I/O pins individually. This is used to slow the rise time

of the pins found to be generating external noise. In general, it is acceptable to reduce the rise time of all pins to the minimum and only increase those that demand a slightly faster time. In this case there are no signals that require anything but the minimum.

2.5 FPGA fit optimisation

The Altera Quartus FPGA development environment provides a software phase called a device-fitter which is used to place and optimise the layout of the logic in the FPGA. During the fitting process a programming scheme is generated to place the logic and to make the desired connections between the functions. The main strategy is to place dependent logic functions together within the device to maximise connectivity. There are also a number of parameters that can be used to drive the fitting process more aggressively. These are used to force the fitter to minimise delays between logic elements, which then reduces the radiated noise from the FPGA.

2.6 RF to FPGA Interface

It is important from a digital design viewpoint in the FPGA that the minimum number of system clocks be used. Although different clock schemes can easily be accommodated, in this case it is undesirable to do so because of the risk of interference products generating mixed in-band signals that can affect the IF chain in the front end down converter. The system clock used in this case is the 40MHz Low Voltage Differential Signal (LVDS) output from the GP2015, which is a relatively clean sine wave. The GP2015 is normally AC coupled but in this case it provides some LVDS bias to the FPGA input, as shown in **Figure 2.**

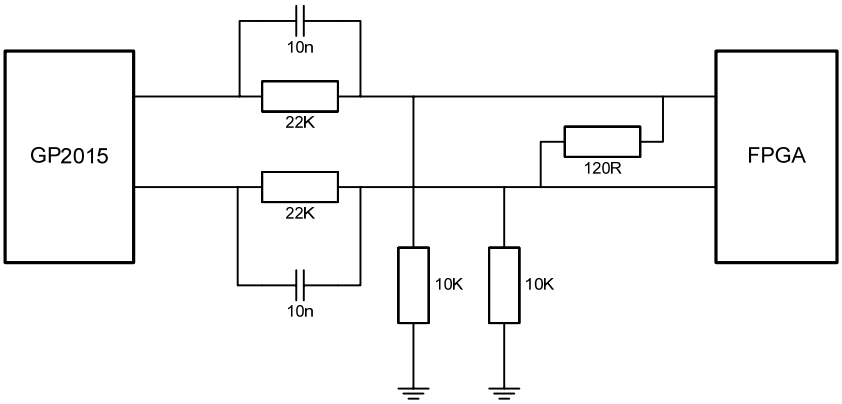

Figure 2. LVDS clock interface

A few of the RF front end control signals generated from within the FPGA needed careful attention to filtering to prevent digital noise passing through into the RF area. In this case a simple low pass resistor capacitor filter is used.

2.7 Reference oscillator

A TCXO reference oscillator module is used to provide a 10MHz AC coupled signal to the GP2015. This oscillator is fed from a separate low-noise low-dropout voltage regulator giving a very clean low noise power supply. The regulator reduces the 5volt regulated supply down to 3 volts further reducing the effect of upstream power supply fluctuations. The aim is to minimise power supply related frequency variations which may appear as a Doppler shift in the measured GPS signal.

3. TEST RESULTS

Tests were carried out to compare a commercially available OEM GPS receiver (Novatel Superstar II [5]) that uses the same GP2015 RF front end chip and the new Namuru receiver. Measurements were taken with a spectrum analyser at the IF output test pin of the GP2015 in both cases. The results show that the Superstar II (See **Figure 3**) contains a number of digital noise spikes both in and out of band that are 5 to 10 dBm greater than the FPGA based receiver (See **Figure 4**) operating under the same conditions.

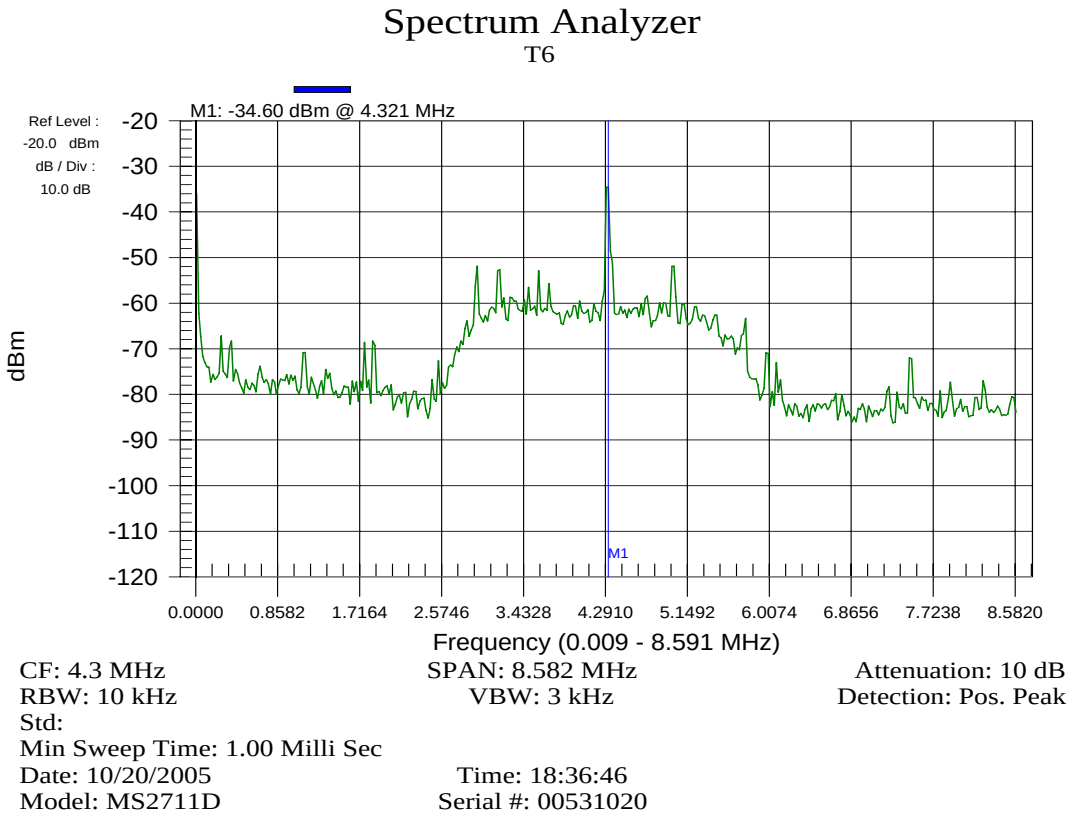

Figure 3. Superstar II receiver with L1 signal at -96dBm

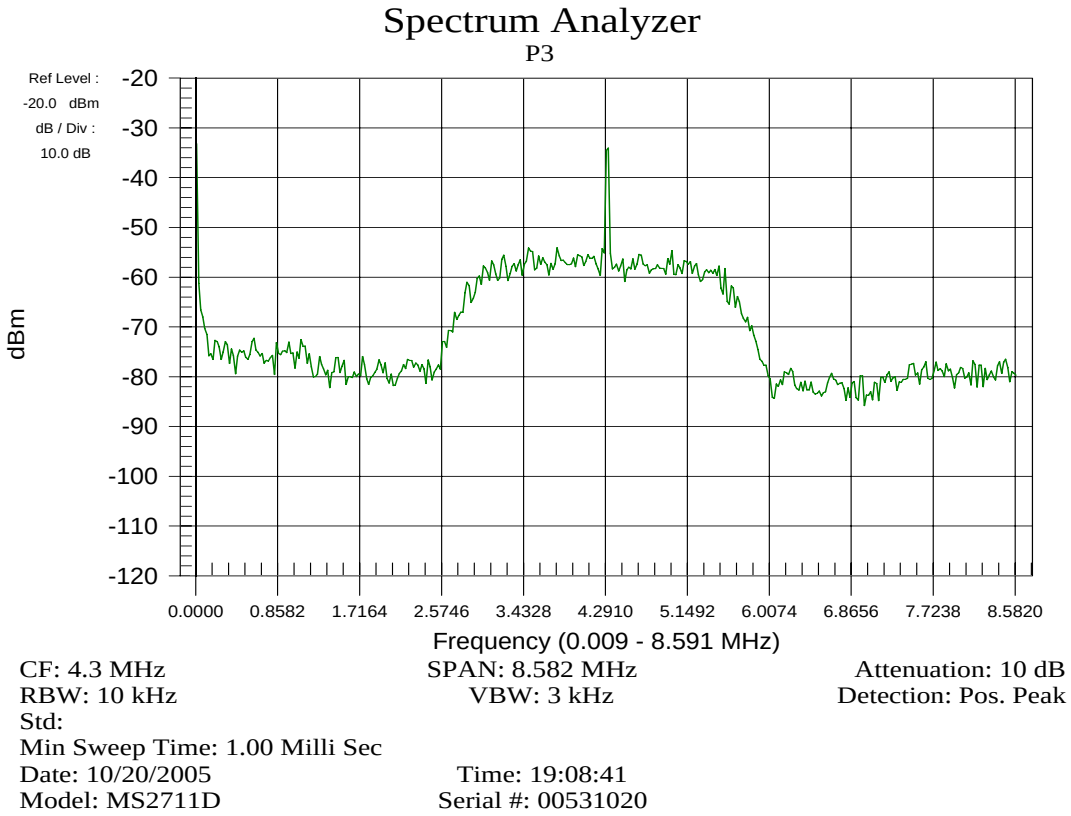

Figure 3. Namuru receiver with L1 signal at -96dBm

4. THE EXTENDED RF FRONT END

Although the L2 GPS frequency (1227.6 MHz) has always been available, it has been largely restricted to military and specialised survey applications. Therefore many commercial GPS receivers are designed for single frequency L1 use only. Recently a GPS modernisation plan for NAVSTAR [6] has proposed new signals for civil use on the L2 frequency and an additional new L5 frequency [7],[8]. With this in mind the RF front end of the Namuru receiver is being extended to allow processing of these new signals.

Since L2 RF front end ASIC devices are not readily available yet, a different approach is being undertaken to introduce the L2 signal into the RF chain combined with the L1 signal in the GP2015 (See **Figure 5**). The Phase Locked Loop (PLL) is required to be high performance and low noise. Division of the GP2015 40MHz reference by 2000 yields a reference frequency of 20KHz. The internal loop division will be 17391 to lock 347.82MHz to the reference. This scheme preserves the phase relationship of any Doppler shifts observed in both L1 and L2 because the reference oscillator is common. A similar scheme is under investigation to access the new L5 signal which is not yet available.

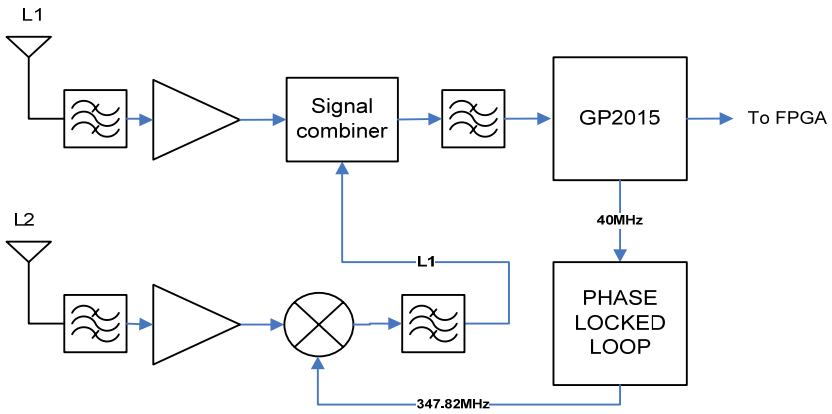

Figure 5. L2 Front end converter

5. CONCLUDING REMARKS

It is especially important to have stability and low noise performance with signal processing research in mind. It has been shown that there are challenges in the design of a GPS receiver that can be overcome with careful attention to specific areas to improve the quality of the measured signal. The FPGA provides a very flexible platform for prototyping and development of baseband signal processing. Planned future enhancement work on the receiver platform include the addition of different interfaces and the design of extra RF front end options for other proposed new GPS signals.

ACKNOWLEDGEMENTS

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