An Application Specific Integrated Circuit Implementation of a Multiple Correlator for UWB Radio Applications

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Abstract – Time Domain Corporation (TDC) has advanced their development of Ultra Wideband (UWB) technology to the point of having designed and produced an Application Specific Integrated Circuit (ASIC) solution for the correlator function in their UWB radio architecture. This paper describes the implementation of an ASIC multiple correlator for UWB radio applications up to 3.0 GHz. The topics covered in this paper include: A brief overview of UWB radio technology, typical UWB receiver system architecture, correlator requirements, Implementation of the ASIC multiple correlator, Preliminary performance data, Future developments, Conclusion:

OVERVIEW OF ULTRA WIDEBAND RADIO TECHNOLOGY

Ultra Wideband radio technology departs from conventional narrowband radio and spread-spectrum technologies in that the half-power bandwidth of the signal is typically from 25 to 100% of the center frequency. This wide bandwidth is a result of the fact that instead of transmitting a continuous carrier wave modulated with information or with information combined with a spread code, which determines the bandwidth of the signal, a UWB radio transmits a series of very narrow impulses. In the TDC implementation of UWB these impulses take the form of a single cycle, or monocycle having pulse widths less than 1 ns. These short time-domain impulses transformed into the frequency domain result in the ultra wideband spectrum of UWB radio (Fig.1).

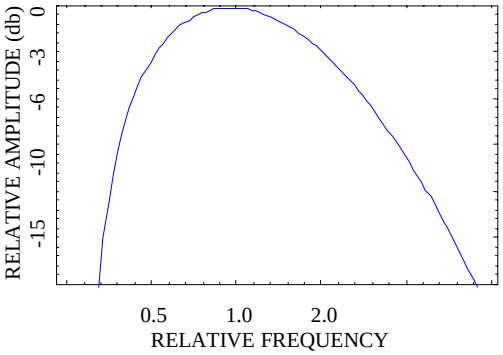

Fig. 1 UWB Spectrum

In the TDC implementation of UWB, information is conveyed by altering the timing of the individual impulses, a form of pulse-position modulation. Fig. 2 illustrates this concept The series of impulses is transmitted at a repetition rate of up to several Megahertz. To convey information, the timing of individual pulses is altered to be either early or late corresponding to a digital "one" or "zero".

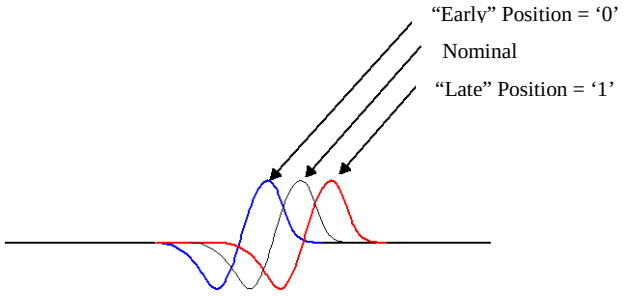

Fig. 2 Information Modulation

TDC refers to this time shifting of the impulse rate as Time-Modulated Ultra Wideband (TM-UWB). To further improve performance, TDC UWB radio technology adds a pseudo-random code to the information which transforms the spectrum of the transmitted signal from a series of regulary spaced discrete frequency components into a random spectrum with noise-like characteristics. The task of the receiver in a TM-UWB radio system is to synchronize to the repetition rate of the transmitted signal, recover the energy in the narrow transmitted impulses, strip off the pseudo-random coding and demodulate the time-modulated information content.

Ultra wideband radio has a distinct advantage over narrowband radio systems in resistance to signal degradation by multipath propagation. In environments having reflecting objects, the continuous carriers of narrowband systems are susceptible to destructive interference due to multipath signals. In a UWB radio system, the multipath signal energy arrives at a different time than the direct path energy and cannot create destructive interference. Moreover, a multiple correlator system can with high probability recover this multipath energy to enhance system performance.

UWB RECEIVER ARCHITECTURE

In order to understand the following sections, we consider here a typical UWB receiver architecture implemented by TDC. Fig. 3 is a block diagram of the TDC UWB receiver

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architecture. The main subsystems are the correlator module, the baseband module and the timing module.

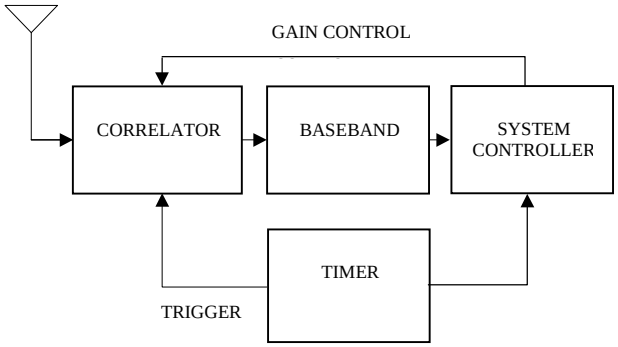

Fig. 3 UWB receiver block diagram

The function of the correlator module is to recover the energy in the transmitted impulses and present a representative signal to the baseband module. The baseband module performs the functions of pulse integration, timing offset during synchronization and reconstruction of the information signal. The timing module generates the precision master clock for all signal processing operations and provides the facility for the baseband module to time-shift the trigger signal to the correlator for synchronization. Once synchronization is achieved the pseudo-random code is included in the timing signal to the correlator which strips off the transmitted signals pseudo-random coding. At this point the correlator output signal contains the information modulation and a D.C. component. In the TDC UWB radio system implementation the timer – correlator combination provides the critical element for reception of the time-modulated ultra wideband signal.

ASIC CORRELATOR REQUIREMENTS

The performance requirements for the ASIC correlator were based on previous system designs which were implemented with correlators constructed from discrete components. Performance requirements for an integrated circuit implementation were determined to be as follows.

- Maximum achievable sensitivity, limited by noise factor of realizable devices. NF = 5db to 6db.
- Dynamic range of 60db, minimum.
- Gain control range of 30db.
- Jitter and dispersion added to the timing signal, <30 pS p-p.
- Triple correlator cell configuration to facilitate implementation of multipath recovery architecture and rake receiver architectures.
- Capability to operate up to 3GHz RF input.
- D.C. coupling to support code lock and tracking.
- Compatibility with TDC ASIC timer module and baseband module (differential signal interfaces).
- Operation over –40 to +85 ^{o}C temperature range.
- Low power consumption to facilitate design of battery powered equipment.

IMPLEMENTATION OF THE APPLICATION SPECIFIC INTEGRATED CIRCUIT CORRELATOR

It is possible to receive impulse transmissions by utilizing a simple crystal-video receiver. However this type of receiver is unsuitable for high-performance radio systems due to inability to achieve processing gain and lack of interference rejection.

The correlator described in this paper is a much more sophisticated approach to the reception of UWB signals. In the ASIC correlator a precisely timed template pulse is used to control a sampling gate. The timing of this template signal is adjusted by the radio system to coincide with the transmitted impulse. When synchronization of the receiver to the transmitter is achieved the spectrum is sampled only at those brief points in time when transmitted energy is actually available. The small sampling interval in relation to the larger pulse repetition interval provides processing gain in the system. The pseudo-random coding applied to the template to strip off the transmitter encoding decorrelates jamming signals.

The basic architecture of the correlator used by TDC is shown in Fig. 4. This architecture incorporates a Variable Gain Amplifier (VGA) which is a low-noise gain stage with facilities for automatic gain control. This amplifier determines the system noise figure and the capability to reduce the gain increases the system dynamic range by the amount of the gain reduction. Associated with the VGA is a power detector, which provides input to the gain control loop. Following the VGA are three identical correlator cells.

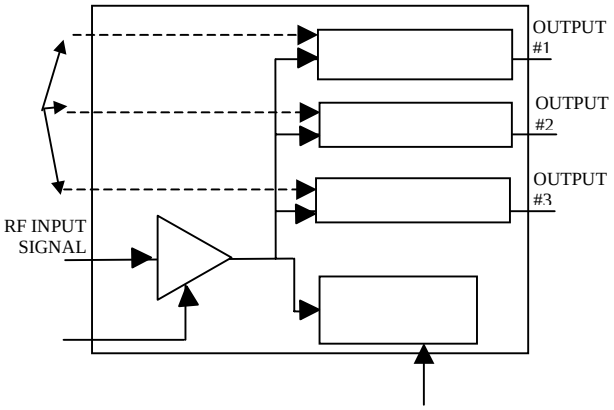

Fig. 4 ASIC Correlator Block Diagram

Each of the multiple correlator cells consists of a sampling gate and template generator followed by a track and hold circuit as shown in Fig. 5.

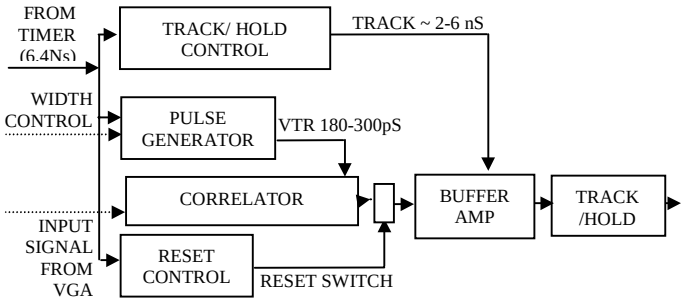

Fig. 5 Correlator Cell Block Diagram

While the function of the VGA is straightforward and easily understood, the functioning of the sampling gate and its associated track and hold stage requires more elaboration. Fig. 6 illustrates the operation of the sampling or correlation process. The timer input signal is processed by the pulse generator to produce a narrow template pulse, nominally 250 ps in width. A DC width control signal allows the template width to be varied to optimize signal sampling. When the template is synchronized to the transmitted signal each sampled pulse produces a short correlator output pulse. The short duration of this pulse requires further processing of the signal. The narrow pulse output from the correlator is processed by a track and hold circuit which produces a wider pulse at the level of the sampled signal pulse for processing by the A/D converter on the baseband module. To assure that the amplitude of the next pulse is not corrupted by residual energy from the preceding pulse, a reset function zeroes the correlator output after the track and hold captures the amplitude information.

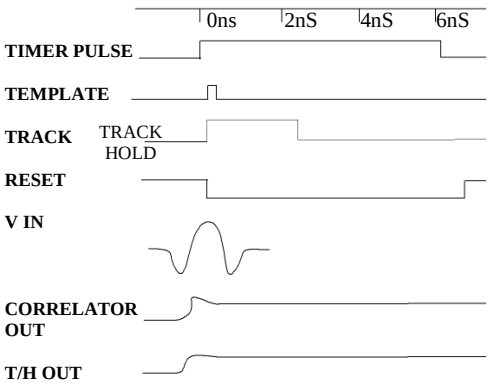

Fig. 6 ASIC Timing Diagram

This ASIC device has been realized as a 3.0 mm by 3.8 mm flip-chip die using Silicon-Germanium (SiGe) technology. In this ASIC device the internal timing requirements and the 1 to 3 GHz operating frequency dictate the need for transistors having a minimum ft of 40 GHz. Additionally, the complexity of the device requires a low power technology to limit total power dissipation. SiGe offers all of these attributes and is easily implemented in conventional CMOS integrated circuit production facilities making it very cost effective.

The major challenge in the development of the ASIC correlator was the development of a design for a correlator cell operating with a 200 ps sampling template at millivolt signal input levels and producing a good output signal to noise ratio. In the design of the device careful attention was given to balancing in the sampler and controlling spurious energy feedthrough from the input and from the template to the output. The entire signal processing path from the VGA input to the baseband output and the timing circuitry uses a balanced topology.

Fig. 7 is a photograph of the ASIC die mounted on a printed wiring board designed to be the test platform for design verification and device characterization. At this time prototype correlator modules for application in systems are being constructed using this test module while work to define and implement the final device packaging is underway.

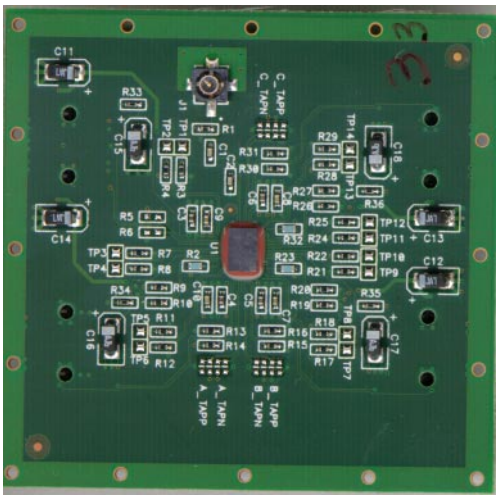

Fig. 7 ASIC test module photo

PERFORMANCE DATA

Characterization of the device is currently underway. Initial performance data taken from the first group of devices is as follows.

Sensitivity versus frequency

Frequency (GHz)	Input for 10db S+N/N (dbm)
1.0	-75.5
2.0	-76.2
3.0	-64.6

Noise figure of VGA

Frequency (GHz)	Noise Figure (db)
1.0	32
2.0	33
3.0	43

Dynamic range (p1db)

Frequency (GHz)	*Input at –1db output (dbm)
1.0	-12/-35
2.0	-12/-34.6
3.0	-10/-32

*Minimum gain / Maximum gain

Isolation between correlator cells

Cell pair	Isolation (db)
A-B	> 40
A-C	> 40
B-C	> 40

Template jitter and dispersion

Trigger (MHz)	P-P jitter* (pS)	Trigger-out delay* (pS)
5.0	< 20	< 20
10.0	< 20	< 20

*Limit of measuring instrumentation.

FUTURE DEVELOPMENTS

Future work will concentrate in two areas. Efforts to further reduce power consumption of the ASIC, for battery powered equipment and extension of the operating frequency range to address systems operating at higher frequencies.

CONCLUSION

Implementation of critical functions as integrated circuits is the only way to achieve the necessary performance, repeatability, cost and power goals for development of practical TM-UWB devices. The integrated circuit correlator described in this paper and the associated timer integrated circuit mark the move of TM-UWB development from a brassboard technology demonstration phase to the product design phase.

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REFERENCES

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