Notes on DPLL[*]

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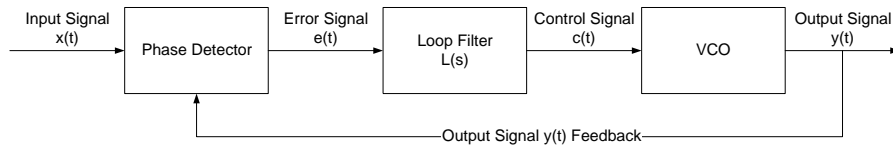
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Figure 1: Structure of a PLL.

1 Digital Phase Locked Loop (DPLL)

1.1 Continuous-time Phase Locked Loop

Figure 1 shows the general structure of a Phase Locked Loop (PLL)[1]. A generic PLL consists of a phase detector, a loop £lter, and a voltage-controlled oscillator (VCO). The phase detector produces the error signal that measures the difference between the input and output of the PLL. The loop £lter averages the error and generates the control signal to the VCO to produce the output signal.

Usually the input and output signals of the PLL are sinusoids with input

$$x(t) = A_x \cos[2\pi f_c t + \phi(t)]$$

and output

$$y(t) = A_y \sin\left[2\pi f_c t + \hat{\phi}(t)\right]$$

After an ideal phase detector, the output error signal is

$$e(t) = \phi(t) - \hat{\phi}(t)$$

The loop £lter is characterized in s-domain (Laplace transform) as

$$C(s) = L(s)E(s)$$

where $E(s)$ corresponds to the error signal $e(t)$, $L(s)$ is the transfer function of the loop £lter, and $C(s)$ corresponds to the control signal $c(t)$. The VCO is basically a sinusoidal signal generator with an instantaneous carrier phase given by

$$2\pi f_c t + \hat{\phi}(t) = 2\pi f_c t + \int_{-\infty}^{t} c(\tau)d\tau$$

Notice we assume the VCO gain is unity here. Any VCO gain will be lumped into the loop £lter gain. Taking the derivative of the above we have

$$\frac{d\hat{\phi}(t)}{dt} = c(t)$$

or equivalently in s-domain

$$s\hat{\Phi}(s) = C(s)$$

where on the LHS, we assumed $\hat{\phi}(0) = 0$. The loop transfer function is then

$$H(s) = \frac{\hat{\Phi}(s)}{\Phi(s)} = \frac{(1/s)C(s)}{\Phi(s)} = \frac{(1/s)L(s)\left[\Phi(s) - \hat{\Phi}(s)\right]}{\Phi(s)} = \frac{L(s)}{s}\left[1 - H(s)\right]$$

Solving the above, we have

$$H(s) = \frac{L(s)/s}{1 + L(s)/s} = \frac{L(s)}{s + L(s)}$$

A £rst-order PLL is characterized by the loop £lter of the form

$$L(s) = K$$

and the transfer function becomes

$$H(s) = \frac{K}{s + K}$$

If we choose the loop £lter of the form

$$L(s) = K\frac{s + K_1}{s + K_2}$$

the transfer function becomes

$$H(s) = \frac{Ks + KK_1}{s^2 + (K + K_2)s + KK_1}$$

which is a second-order PLL. It is customary to express the denominator of $H(s)$ in the form[2]

$$s^2 + 2\eta\omega_n s + \omega_n^2$$

where η is called the *loop damping factor* and ω_n is called the natural frequency of the loop. It is clear that

$$\omega_n = \sqrt{KK_1}$$
$$\eta = \frac{K + K_2}{2\sqrt{KK_1}}$$

the loop transfer function becomes

$$H(s) = \frac{Ks + \omega_n^2}{s^2 + 2\eta\omega_n s + \omega_n^2}$$

When $K_2 = 0$, we have a special second-order PLL with the loop £lter

$$L(s) = K\frac{s + K_1}{s} \tag{1}$$

and transfer function

$$H(s) = \frac{Ks + KK_1}{s^2 + Ks + KK_1} = \frac{2\eta\omega_n s + \omega_n^2}{s^2 + 2\eta\omega_n s + \omega_n^2} \tag{2}$$
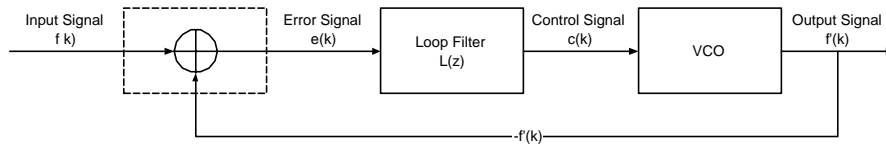
2

Figure 2: General structure of a DPLL.

and the natural frequency and damping factor are

$$\omega_n = \sqrt{KK_1}$$
$$\eta = \frac{1}{2}\sqrt{\frac{K}{K_1}}$$

respectively.

It is often useful to know the steady-state operating point of PLL. The steady-state phase error is de£ned to be

$$e_{ss} = \lim_{t \to \infty} e(t)$$

Using the £nal value thereom of Laplace transform, we have

$$e_{ss} = \lim_{s \to 0} sE(s) = \lim_{s \to 0} s\Phi(s)\left[1 - H(s)\right] = \lim_{s \to 0} \frac{s^2\Phi(s)}{s + L(s)}$$

1.2   General structure of DPLL

Figure 2 shows the structure of a Digital Phase Locked Loop. The phase detector is a simple substractor. The error signal is

$$e(k) = \phi(k) - \hat{\phi}(k)$$

or in z-domain

$$E(z) = \Phi(z) - \hat{\Phi}(z)$$

Analogous to the differential equation for the VCO in the continuous PLL, we write the difference equation

$$\hat{\phi}(k+1) - \hat{\phi}(k) = c(k)$$

for the VCO in the DPLL. In z-domain, the above becomes

$$(z-1)\hat{\Phi}(z) = C(z) = L(z)E(z) = L(z)\left[\Phi(z) - \hat{\Phi}(z)\right]$$

which can be reorganized to give the transfer function

$$H(z) = \frac{L(z)}{L(z) + z - 1}$$

The steady state error is calculated as

$$e_{ss} = \lim_{k \to \infty} e(k) = \lim_{z \to 1}(z-1)E(z) = \lim_{z \to 1} \frac{(z-1)^2\Phi(z)}{L(z) + z - 1} \tag{3}$$

3

1.3 First-order DPLL

For the £rst-order DPLL,

$$L(z) = K$$

the transfer function becomes

$$H(z) = \frac{K}{K + z - 1}$$

The £rst-order DPLL is not quite suited for correcting the phase error caused by residual frequency offset as discussed in Section **??**.

For example, if we assume the input sequence is of the form

$$\phi(n) = \epsilon_0 n$$

i.e. a residual frequency offset causing linear phase increment. To £nd out the z-transform of the sequence, we notice that the above sequence is expressed by the difference equation

$$\phi(k + 1) - \phi(k) = \epsilon_0 \quad k \geq 0$$

and

$$\phi(k) = 0 \quad k \leq 0$$

The z-transform of the RHS of the difference equation is

$$\epsilon_0 \sum_{n=0}^{\infty} \frac{1}{z^n} = \epsilon_0 \frac{z}{z - 1}$$

Performing z-transform on both sides of the difference equation yields

$$z\Phi(z) - \Phi(z) = \epsilon_0 \frac{z}{z - 1}$$

and thus the z-transform of the input sequence $\phi(n)$ is

$$\Phi(z) = \epsilon_0 \frac{z}{(z - 1)^2}$$

Substituting the sequence z-domain expression into the DPLL steady state error expression (3), we have

$$e_{ss} = \lim_{z \to 1} \frac{(z - 1)^2 \epsilon_0 \frac{z}{(z-1)^2}}{K + z - 1} = \frac{\epsilon_0}{K}$$

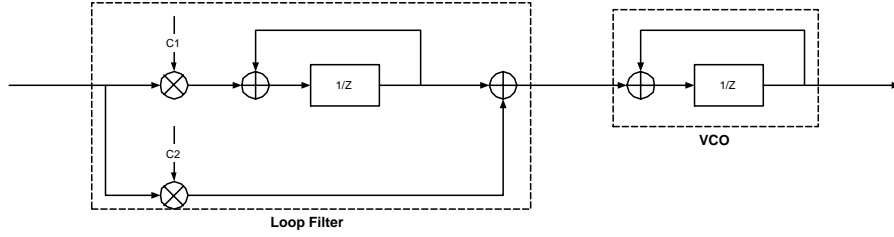The steady state error is non-zero but it can be reduced by increasing the loop gain K.

Figure 3: Second-order DPLL loop filter and VCO.

1.4 Second-order DPLL

1.4.1 Second-order DPLL structure

Noticing the discrete domain equivalent of s is $z-1$, we can construct a special second-order DPLL similar to the PLL discussed before, whose loop filter is, similar to (1),

$$L(z) = K\frac{(z-1) + K_1}{(z-1)}$$

and whose transfer function is, similar to (2),

$$H(z) = \frac{K(z-1) + KK_1}{(z-1)^2 + K(z-1) + KK_1}$$

The filter parameters can be matched with those used in [3] through

$$\begin{cases} K = C_2 \\ K_1 = C_1/C_2 \end{cases} \quad \text{i.e.} \quad \begin{cases} C_1 = KK_1 \\ C_2 = K \end{cases}$$

and the transfer function becomes

$$H(z) = \frac{C_2(z-1) + C_1}{(z-1)^2 + C_2(z-1) + C_1} \tag{4}$$

Figure 3 shows the block diagram of the second-order DPLL.

Now if the input is

$$\phi(n) = \epsilon_0 n$$

the steady state error is

$$e_{ss} = \lim_{z \to 1} \frac{(z-1)^2 \epsilon_0 \frac{z}{(z-1)^2}}{K\left(1 + \frac{1}{z-1}K_1\right) + (z-1)} = \lim_{z \to 1} \frac{\epsilon_0 z(z-1)}{(z-1)^2 + K(z-1) + KK_1} = 0$$

To express the DPLL in term natural frequency ω_n and damping factor η, we define

$$\begin{cases} C_1 = \omega_n^2 \\ C_2 = 2\eta\omega_n \end{cases} \quad \text{i.e.} \quad \begin{cases} \omega_n = \sqrt{C_1} \\ \eta = \dfrac{C_2}{2\sqrt{C_1}} \end{cases} \tag{5}$$

5

Notice here we require C_1 to be positive which as discussed later is a prerequisite for a stable DPLL. With the de£nition, we can express the DPLL transfer function as

$$H(z) = \frac{2\eta\omega_n(z-1) + \omega_n^2}{(z-1)^2 + 2\eta\omega_n(z-1) + \omega_n^2}$$

1.4.2 Second-order DPLL stable condition

To have a stable DPLL, all its poles must reside in the unit circle. The poles can be found by solving the equation in the denominator of $H(z)$,

$$(z-1)^2 + C_2(z-1) + C_1 = 0$$

yielding the soluation of the form

$$z = 1 + \frac{-C_2 \pm \sqrt{C_2^2 - 4C_1}}{2} = \frac{2 - C_2 \pm \sqrt{C_2^2 - 4C_1}}{2}$$

When

$$\frac{C_2^2}{4} > C_1$$

the solution is real and we require

$$-1 < \frac{2 - C_2 \pm \sqrt{C_2^2 - 4C_1}}{2} < 1$$

Noticing that we only need to make the bigger pole to be less 1 and the smaller pole to be bigger than -1, the above inequality is reduced to

$$\frac{2 - C_2 + \sqrt{C_2^2 - 4C_1}}{2} < 1$$
$$\frac{2 - C_2 - \sqrt{C_2^2 - 4C_1}}{2} > -1$$

From the £rst of the two inequalities, we £nd

$$0 < \sqrt{C_2^2 - 4C_1} < C_2$$

and futher

$$C_1 > 0$$

From the second of the two inequalities, we £nd

$$4 - C_2 > \sqrt{C_2^2 - 4C_1} > 0 \quad \Rightarrow \quad C_2 < 4$$

and further

$$C_1 > 2C_2 - 4$$

Combine all above we have

$$\frac{C_2^2}{4} > C_1$$
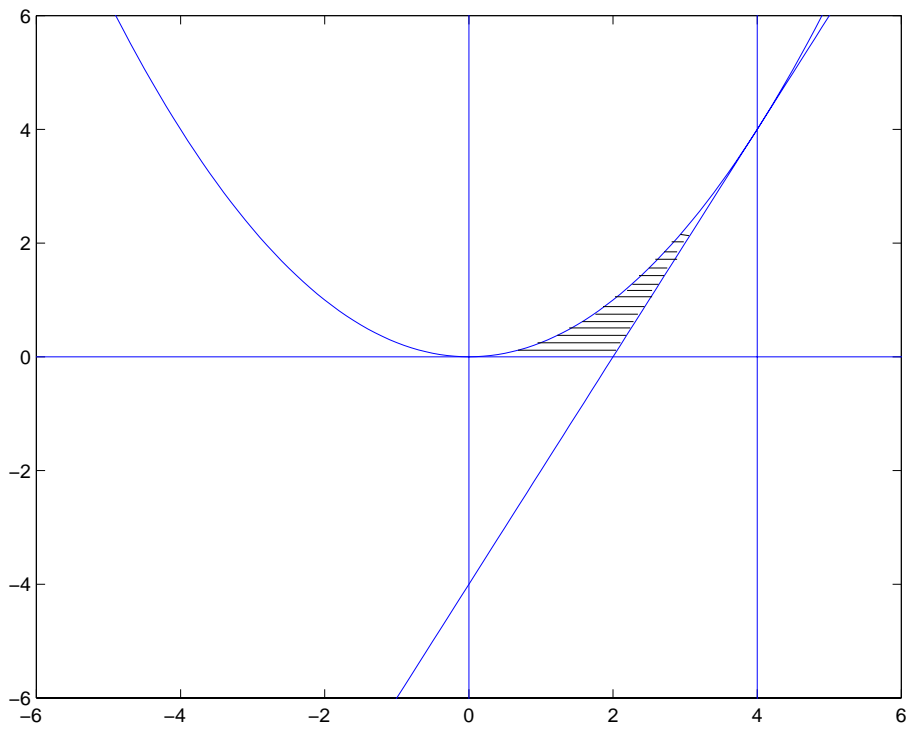$$0 < C_2 < 4$$
$$C_1 > 0$$
$$C_1 > 2C_2 - 4$$

6

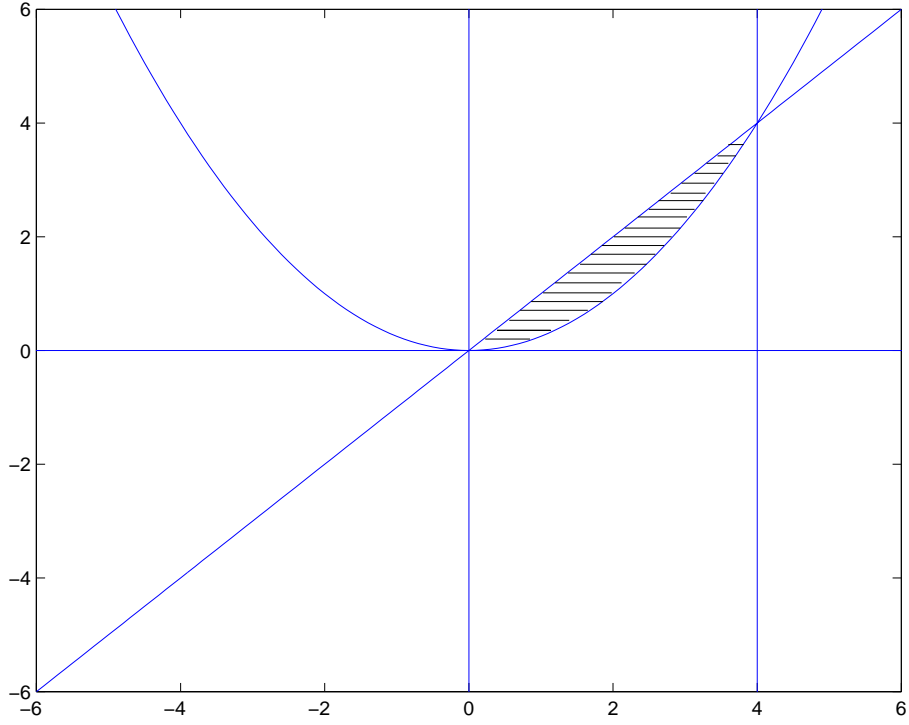Figure 4: Second-order DPLL real solution region. Horizontal axis is C_2. Vertical axis is C_1.

Figure 5: Second-order DPLL imaginary solution region. Horizontal axis is C_2. Vertical axis is C_1.

The shaded region in Figure 4 shows the solution region.

When

$$\frac{C_2^2}{4} \leq C_1$$

the poles are not on the real axis and we require

$$\left| \frac{2 - C_2 \pm j\sqrt{4C_1 - C_2^2}}{2} \right| < 1$$

which is equivalent to

$$(2 - C_2)^2 + \left(4C_1 - C_2^2\right) < 4$$

reducing to

$$C_1 < C_2$$

The solution is shown as the shaded region in Figure 5.

Combining the two graphs, we £nd the overall solution for a stable second-order DPLL in Figure 6. Mathematically, the DPLL parameters C_1 and C_2 must satisfy

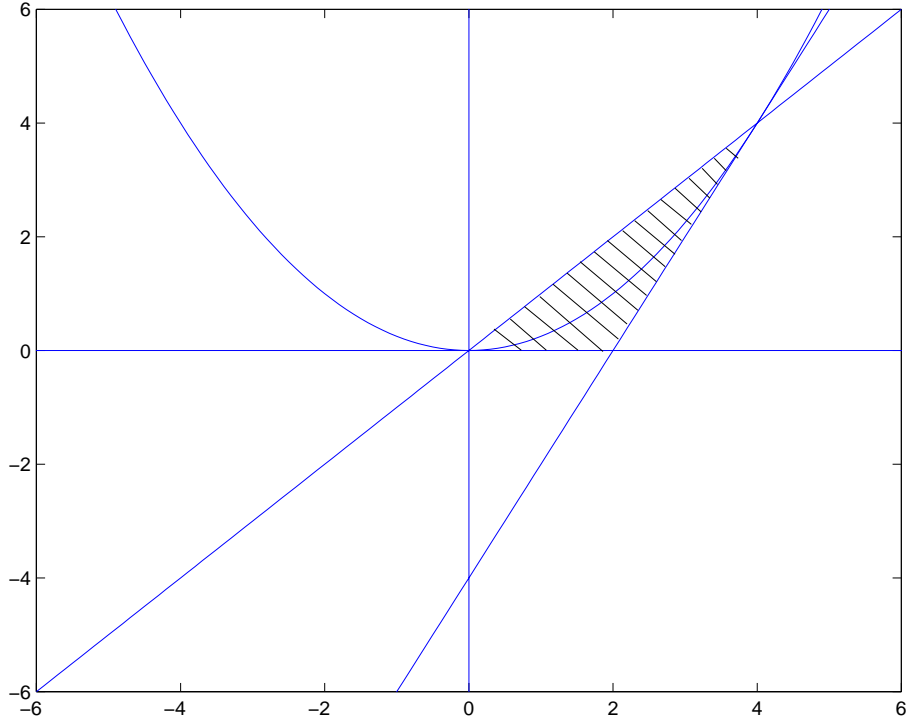$$C_1 > 0, C_1 > 2C_2 - 4, C_1 < C_2$$

8

Figure 6: Second-order DPLL solution region. Horizontal axis is C_2. Vertical axis is C_1.

Referring to (5), we can also express everything in terms of natural frequency and damping factor. Here since C_1 and C_2 are both positive, ω_n and η must be of the same sign. It doesn't matter whether both of them are negative or positive because the transfer function only depends on ω_n^2 and $2\eta\omega_n$. We require both of them to be positive.

For the £rst case, we have $\eta > 1$, we have the stable condition

$$\omega_n > 0$$
$$\eta > 1$$
$$\eta\omega_n < 2$$
$$\omega_n^2 + 4 > 4\eta\omega_n$$

From the third inequality, we have

$$\omega_n < 2/\eta < 2$$

From the last inequality, we have
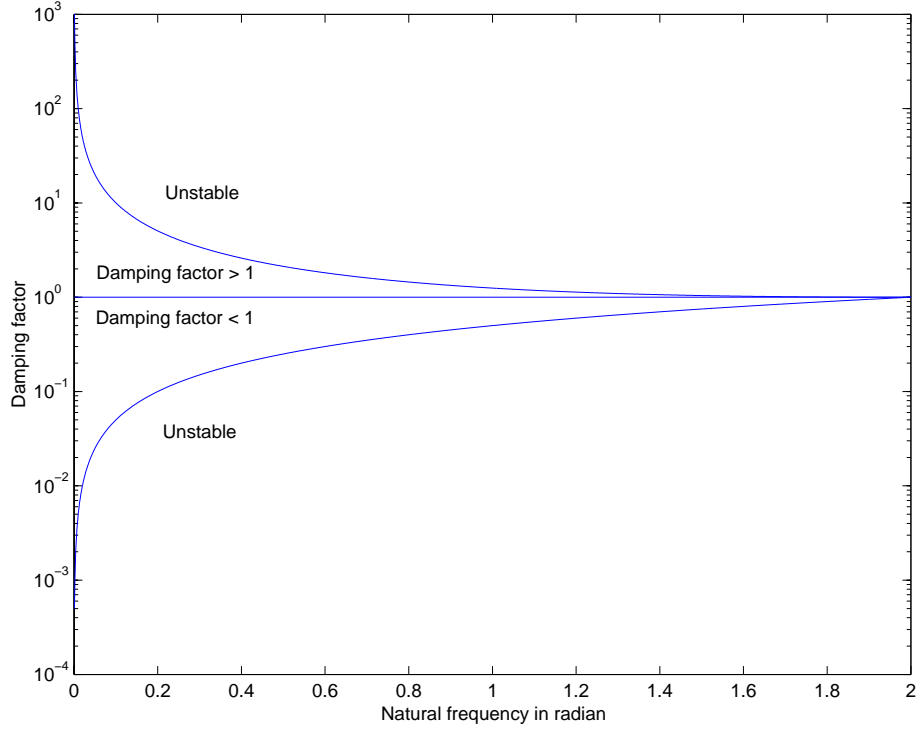
$$\eta\omega_n < \frac{\omega_n^2}{4} + 1$$

9

Figure 7: Second-order DPLL solution region in terms of natural frequency ω_n and dampling factor η.

which combined with the condition $\omega_n < 2$ supercedes the second inequality above. We can thus rewrite the condition as

$$
\begin{aligned}
\eta &> 1 \\
0 < \omega_n &< 2 \\
\eta\omega_n &< \frac{\omega_n^2}{4} + 1
\end{aligned}
\tag{6}
$$

For the second case, we have the stable condition

$$
\begin{aligned}
\eta &\leq 1 \\
0 < \omega_n &< 2\eta
\end{aligned}
\tag{7}
$$

The solution region in terms of natural frequency and damping factor is shown in Figure 7.

References

[1] Edward A. Lee and David G. Messerschmit. *Digital Communications*. Kluwer Academic Publishers, second edition, 1994.

[2] John G. Proakis. *Digital Communications*. Electrical Engineering Series. McGraw-Hill, third edition, 1995.

[3] Y. R. Shayan and T. Le-Ngoc. All digital phase-locked loop: concepts, design and application. *IEEE Proc.*, 136(1), February 1989.

[4] Christian Stimming. Frequency offset tracking in mcma systems. Technical report, Berkeley Wireless Research Center, May 2001.