Design Of High Frequency Digital Phase Locked Loops

Brian Daniels$^{\phi}$ and Ronan Farrell*

School of Electronic Engineering,
National University of Ireland, Maynooth
IRELAND
*E-mail:$^{\phi}$bdaniels@eeng.nuim.ie, *rfarrell@eeng.nuim.ie*

This paper considers the stability of high order Charge Pump Phase Lock Loop (CP-PLL), proposing a novel means of identifying stable regions for such systems. Traditional design techniques are inefficient for high frequency, high order CP-PLL systems. This paper proposes an accurate and efficient means of identifying stable regions for 2nd and 3rd order high frequency (> 1GHz) CP-PLL. Using exact non-linear CP-PLL responses it is shown that the proposed stability technique is a significant improvement over existing linear methods.

Keywords – Stability, Charge Pump, Phase Locked Loop, High Frequency.

I INTRODUCTION

PLL systems are used to create a robust and noiseless oscillating signal from a noisy oscillator. First order systems with no loop filter are the simplest form of PLL system, these have no stability concerns and lock to a signal quickly but are noisy. Second order systems include a loop filter on the output of the phase frequency detector (PFD) to attenuate the jitter on the output signal of the voltage controlled oscillator (VCO). However second order PLLs have stability issues and the designer needs to trade-off between the noise reduction in the loop and the stability of the system. Higher order systems are increasingly less stable as the order is increased, but provide attenuation of the frequency jumps inherent in the second order PLL as well as better attenuation of the in-band noise. Traditionally the second and third order CP-PLLs are designed using linear theory to define a stable region of the CP-PLL, once determined 'rule of thumb' and empirical design are used to ensure the correct transients of this system.

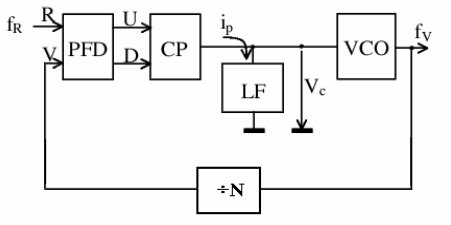


Figure 1: CP-PLL system

This paper proposes a piece-wise linear technique to design stable high frequency CP-PLL systems by identifying stable regions of such systems.

In the next section the traditional techniques of designing the CP-PLL are outlined. In section 3 the proposed technique is introduced. In section 4 the proposed technique's stability boundaries are determined and, for the second a third order PLLs, are compared to the traditional linear stability boundaries. The stability boundary for the forth order system are also determined. It is shown that the proposed technique is a significant improvement on the traditional method.

II TRADITIONAL DESIGN TECHNIQUES

The Digital PLL of Figure 1 is a non-linear system, the non-linearity lying primarily in the PFD and the VCO and are essential to the PLLs operation. Despite this linear methods such as Gardner's stability criterion [1] are commonly used to identify stable component values of the CP-PLL. These are applied to the non-linear CP-PLL using the justification that the CP-PLL will be less non-linear if the cut-off frequency is restricted to no greater then 1/10th of the reference frequency. To insure the stability of the designed system, empirical design and simulation of the system are used concurrently. This design technique is a cumbersome process due to the initial offhand assumptions made to justify the application of the linear model to the CP-PLL. Non-linear stability

criteria have only occasionally been applied to low order analog PLLs. This is due to the fact that non-linear methods are unwieldy and in particular are not suitable for the stability analysis of complicated high order Digital PLLs.

As mentioned the PLL is a non-linear feedback system, the non-linearities exist in the voltage controlled oscillator, due to saturation and the CP-PFD, due to switching in the PFD. This switching is due to the fact that the output of the CP-PFD moves between states and yields a corresponding output current of $+I_p$, zero, or $-I_p$ amps. Simple transfer function analysis is not directly applicable to time-varying networks. This is overcome for the purpose of justifying the application of linear theory, by considering only the average behaviour of the system over many cycles, this is known as the continuous time approximation [1]. The second linearising assumption is that by ignoring high frequency components of the PFD output signal the PFD can be modeled as a subtractor, making the overall PLL system a negative feedback system, as shown in figure 2.

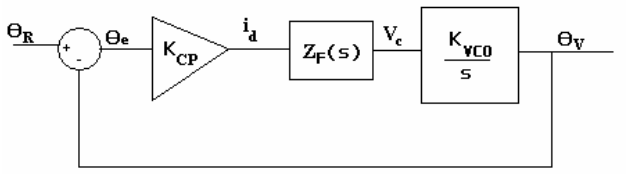


Figure 2: Linear CP-PLL system

From the block diagram of the linearised DPLL of Figure 2, the closed loop system transfer function is calculated as that of equation (1) below, where K_P is the CP gain, K_V is the VCO gain and F(s) is the loop filter transfer function.

$$H_{CL}(s) = \frac{K_P K_V F(s)}{s + K_P K_V F(s)} \quad (1)$$

This linearised S-domain system characteristic equation is used extensively in the literature to identify stable boundaries and stable system component values of the DPLL, in particular Gardner [1], O'Keese [2], Williamson [3] and Banerjee [4].

For the second order PLL system Gardner [1] identifies the stability boundary as shown in equation (2), using the continuous time approximation.

$$K' = \frac{1}{\frac{\pi}{\omega_i \tau_2}\left(1 + \frac{\pi}{\omega_i \tau_2}\right)} \quad (2)$$

A plot of the stability boundary from equation (2) for a defined filter time constant τ_2, and a range of reference frequencies (ω_i radians/second) is shown in Figure 3.

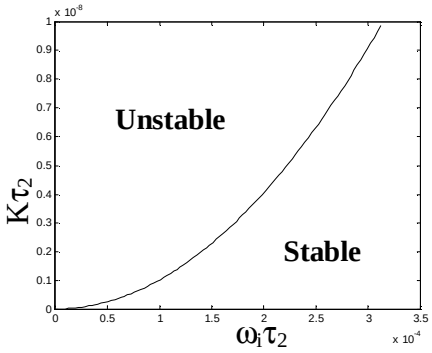


Figure 3: Second order Gardner Stability Boundary

On its own linear stability Criterion such as Gardner's do not define a definitive prediction of stability for the CP-PLL this is due to the inaccuracies introduced while linearising the system. However they do provide a starting point from which empirical design methods are used to choose optimum component values from those suggested by Gardner and to insure that the CP-PLL will operate as expected.

A number of 'rules of thumb' are commonly applied to the design of the DPLL, the most common of these are:

1. The loop filter bandwidth must be no greater then one fifth the reference frequency, and is generally chosen to be a ratio of $1/10^{th}$, this will rationalise the continuous time approximation [2].
2. To obtain some stability margin, the ratio of the reference frequency (ω_i) to the system gain should be chosen in excess of 15 to 20[1].
3. For a third order PLL, the additional ripple capacitor C_3 in figure 4, must be ten times that of the capacitor of the RC filter, C_2, this ensures a loop bandwidth of approximately $1/10^{th}$ that of the reference frequency and a phase margin of at least 40-45 degrees [2,4].

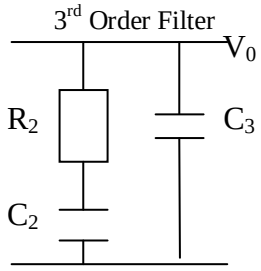


Figure 4: Third and Forth order CP-PLL filter.

III PROPOSED STABILITY CRITERION

If we consider the state space diagram of a typical stable second order DPLL as shown in Figure 5, we see that for a positive initial control voltage (V_C) offset, the system moves in an anticlockwise direction and spirals into the origin. The system stability is related to the rate at which the system

approaches the equilibrium point (0,0). If the system does not approach the equilibrium then the system is unstable. By considering one plane of the state space, the stability of this system may be determined as long as no cycle slips occur. The accuracy of this model depends on the size of reference frequency (F_{REF}) of the DPLL and the size of the initial offset of the control voltage V_C. The larger the value of F_{REF} the smaller the error will be. The occurrence of cycle slips in the PLL is a highly non-linear phenomenon cause by a large offset of the phase error generally due to noise [6]. Using the proposed technique they are avoided by only considering a small initial V_C offset, this keeps the system close to the equilibrium thereby reducing the chance of a slip. If the system is stable then a cycle slip will not cause the PLL to go unstable, in fact it has the effect of reducing the immediate phase error and pushing the loop towards the equilibrium.

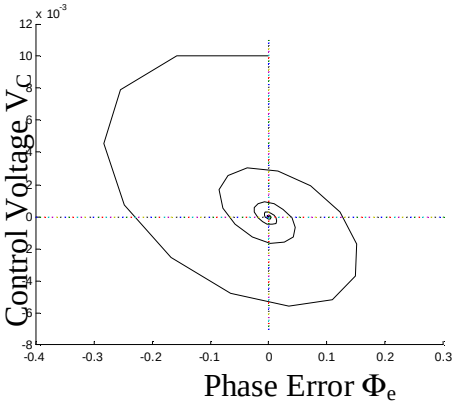


Figure 5: State Space Plot of Stable System

In any time period T_{TOT}, the DPLL operates in the NULL state (or coast state) for a period of T_{coast}, and in the UP or DOWN states (boost state) for a period of T_{boost}, where $T_{TOT} = T_{boost}+T_{coast}$. The time period T_{TOT} is equal to $1/ F_{REF}$. Consider the plot of V_C for this second order system as shown in Figure 6, the time period T_{boost} is calculated as:

$$T_{boost} = \left| \frac{\Phi_e(t_n) T_{TOT}}{2\pi} \right| \quad (3)$$

Where $\Phi_e(t_n)$ is the phase error at time t_n. From this the coast time period is calculated as $T_{coast} = T_{boost}-T_{TOT}$. Once the time periods are calculated, V_C can be calculated from Φ_e using the filter difference equations of the DPLL. For a second order DPLL the control voltage V_C is calculated as from equation (4), where $I_{IN} = I_P Sign(\varphi_e)$ and I_P is the charge pump gain.

$$V_C(t_{n+1}) = V_C(t_n) + \frac{I_{IN} T_{boost}}{C} \quad (4)$$

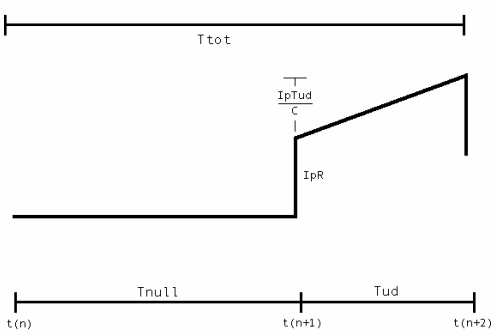


Figure 6: Plot of V_C for period T_{TOT} for Second Order DPLL

The phase error of the DPLL at time $t_{(n+2)}$, where F_{FV0} is the VCO free running frequency, and K_V is the VCO gain, is:

$$\Phi_e(t_{n+1}) = \Phi_e(t_n) + 2\pi\left(T_{TOT}(F_{REF} - F_{FV0}) - \left(K_V \int V_C dt\right)\right) \quad (5)$$

To solve the above equation an estimate of the integral of V_C is required. For the second order PLL, the loop filter is first order, figure 7, therefore first order integration is used, and is calculated as the area under the line as shown in figure 8. For the second order system the integral of VC is determined as:

$$\int V_C dt = T_{TOT} V_C(t_n) + T_{UP} I_{IN} R + \frac{T_{UP}^2 I_{IN}}{2C} \quad (6)$$

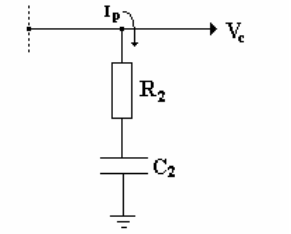
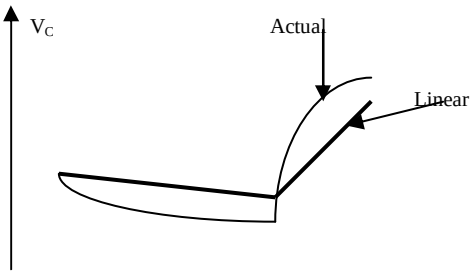


Figure 7: First order filter

For higher order systems equations (4) and (6) need to be recalculated as required for the respective order of loop filter. Unlike the second order case the filter response is non-linear during both the boost state period and the coast state period. The operating can be simplified if a linear response of the filter is used. In charge approximation [6], first order approximation is used along with an iterative technique to accurately model the higher order filters. With this technique a similar method is used except without the iteration. In other words between t(n) and t(n+1) (the coast period) and between t(n+1) and t(n+2) (the boost period) a first order linear approximation of the filter is used, as shown in Figure 8.



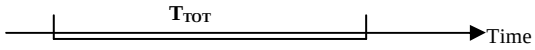


Figure 8: **Calculation of the Integral of V_C**

This can be justified for high frequency systems because for large F_{REF} we get a small T_{TOT}. If $_{TTOT}$ is small then the linear approximation made is small and has little effect on the result. This technique is found to be accurate for frequencies of greater of 1GHz.

The calculation of the higher order equations, instead of (4) and (6), may be simplified by using the charge approximation technique [6] with no iteration, this is described in more detail later. So the shorter the boost period of the PLL, the more accurate the model will be. T_{Boost} can be reduced by using a large F_{REF} and by using a small initial V_C offset, therefore as F_{REF} is indirectly proportional to the time period T, the model will be more accurate at higher frequencies. To determine the state space response of the DPLL equations (4), (5), and (6) need to be iterated over time. A plot of the small signal model (V_C verses Φ_e) of a third order DPLL system iterated while the phase error is less then zero, is shown in Figure 9 for an initial V_C offset of 10mV, and an initial φ_e offset of 0, this is the arc of the state space response in one plane. In this plot the system is stable if $\Delta_1 < \Delta_2$, because the system spirals towards the equilibrium.

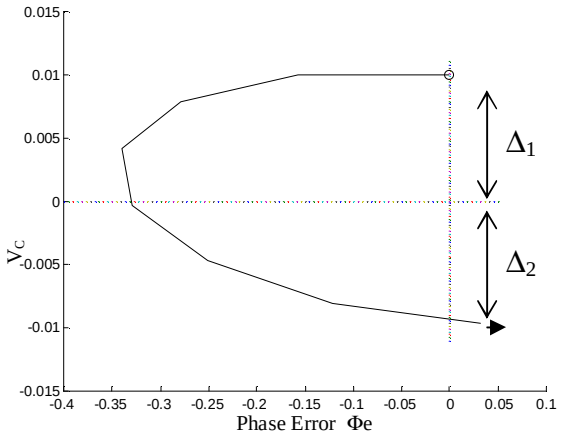


Figure 9: Plot of Arc in One Plane of State Space

An important parameter of this technique is the initial state of the PFD. The initial state will be either the coast state or the boost state. For a V_C step, the PFD state changes immediately to the boost state, therefore for the initial T_{boost} period of T_{TOT}, the system is in the boost state. However for a Φ_e offset, the PFD state is not changed immediately and therefore for the initial T_{coast} time period of T_{TOT}, the system will operate in the coast state.

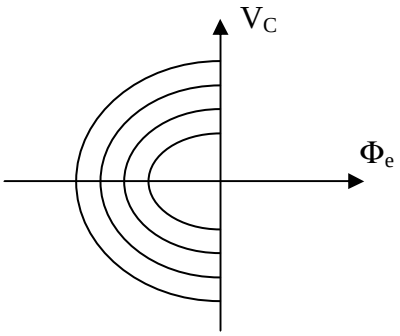


Figure 10: PLL State Space Arcs for a Variety of Intial Offsets

So for any CP-PLL the stability of the system can be quickly and accurately determined using this technique. This system has two properties of interest, firstly for a variety of initial V_C offsets, as in Figure 10, each arc of the state space response does not intersect the other, this shows that the PLL system spirals uniformly into the equilibrium. Secondly the stability boundary of this system is independent of the initial V_C. These two properties give the designer certainty that if one arc in state space of a particular system is determined, this gives an accurate representation of the response of the system regardless of the initial offset or subsequent path through state space. Both these properties are validated in the following subsections.

a) *State Space Curves do not Intersect*

Firstly consider the first period T of curves C_1 and C_2, starting at V_1 and V_2 respectively, as shown in Figure 11. The second order system, described by equations (4), (5), and (6) can be reduced down to the pair of summation equations (7) and (8), where V_O is the initial V_C offset and φ_0 is the initial φ_e offset.

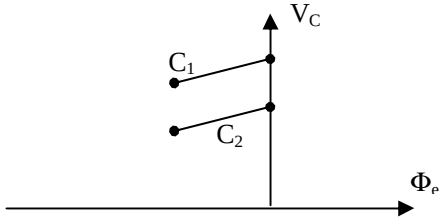


Figure 11: Plot of First Period for two curves

$$V_C(j) = V_0 + \frac{I_P T_{TOT}}{2\pi C} \sum_{i=0}^{j-1} \varphi_e(i) \tag{7}$$

$$\varphi_e(j) = -2\pi K_V T_{TOT} \sum_{i=0}^{j-1} V_C(i) \tag{8}$$

These equations only apply to a second order system with initial phase error of 0, and some positive initial Vo voltage, as in the system plotted in Figure 5. If the slope of C_1 and C_2 are the same then it is intuitive that the curves will never intersect. The slope of C_1 is calculated as:

$$\frac{\Delta_{V_C}}{\Delta_{\Phi_e}} = \frac{-V_1\left(\frac{K_V I_P T^2}{C}\right)}{V_1(2\pi K_V T)} = \frac{-I_P T}{2\pi C}$$

(9)

Note that in equation (9) above the slope of C_1 is calculated from (7) and (8) and is independent of the initial condition V_0. Similarly the curve of C_2 can be shown to be the same as that in equation (8), therefore both curves are parallel to each other. Likewise it can be shown that any two curves with an equal initial condition of φ_0, are parallel regardless of initial V_0. From this it can be concluded that any two curves of a system will not intersect.

b) *Stability is Independent of V_0*

The second order system described by (7) and (8) can again be simplified by substituting equation (8) into equation (7), this results in equation (10).

$$V_C(m) = V_0 - \frac{K_V I_P T_{TOT}^2}{C} \sum_{i=0}^{m-1} \sum_{k=0}^{i-1} \left(1 - K_V I_P R T_{TOT}\right)^{i-j-1} V_C(k)$$

(10)

Where $m = 2\pi / \sqrt{(K_V I_P (4 - K_V I_P R^2 C))/C} + 1$.

From equation (10) the system is stable if $V_0 - |V_C(m)| > 0$, as shown in figure 12.

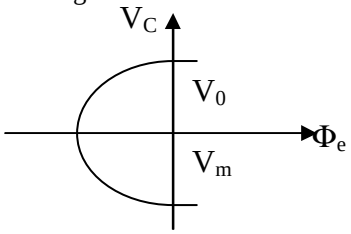


Figure 12: State Space Plot of initial V_0 and final V_m

So the stability boundary is calculated as in equation (11) below.

$$\frac{K_V I_P T^2}{C} \sum_{i=0}^{m-1} \sum_{k=0}^{i-1} \left(1 - K_V I_P R T\right)^{i-k-1} V_C(k) = 2V_0$$

(11)

Consider the first few iterations of m from 0 up to 3, where $A = K_V I_P T^2/C$, $B = 1 - K_V I_P RT$:

0. $V_0 = V_0$
1. $V_1 = V_0$
2. $V_2 = V_0 + AV_0$
3. $V_3 = V_0 + A(V_0(B+1) + V_1) = V_0(1 + A(B+1) + A)$

All subsequent values of m from 4 $\rightarrow\infty$ comprise of previous V_m. In fact any V_m can be reduced to V_0 times a set of A and B equations, such as 3 above, as described in equation (12).

$$V_m = V_0(1 + \mathrm{L} + [A, B]) = V_0 X$$

(12)

It is clear that V_m is the product of V_0 and some function of A's and B's. So going back to equation (11) it is clear that the stability boundary is $V_0 X = 2V_0$, where X is an unknown containing A's and B's. Therefore the boundary is X=2 and is therefore independent V_0, the initial control voltage offset.

For higher order systems it is customary to derive a unique difference equation for each type of filter architecture to replace equations (4) and (6). These difference equations contain differential terms and become increasingly complex as the order of the loop filter increases. Charge approximation [6] reduces this complexity making it possible to derive closed form solutions to high order DPLLs. This is achieved by considering the charge on each capacitor rather then the voltage at each node, and making the assumption that the average current I_{ave} through a capacitor during the period Δ is equal to the current at time t (Figure 13).

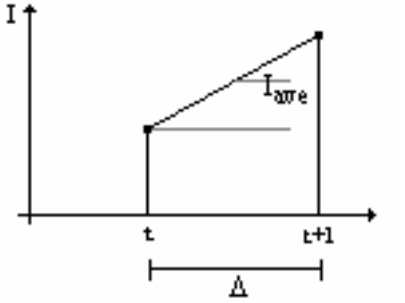


Figure 13: Assumption that current at time t is equal to the average current during Δt

For example in equation (13), to calculate $V_C(t+1)$, the average current I_{ave} during time Δ is unknown and approximated as the initial current at time t, I(t).

$$V_C(t+1) = \frac{\Delta Q_C}{C} = \frac{Q_C(t) + I_{ave}\Delta t}{C} \qquad (13)$$

This simplifies the calculation of V_c, as there are no differential terms, making it significantly easier to increment the model to any arbitrary order. The error introduced is bounded, as it tends to zero as the time interval Δ tends to zero, as shown in Figure 14a and 14b. The time interval Δ is inversely proportional to the frequency so is reduced as the frequency is increased. Therefore as mentioned earlier, the technique is more accurate for higher frequency systems.

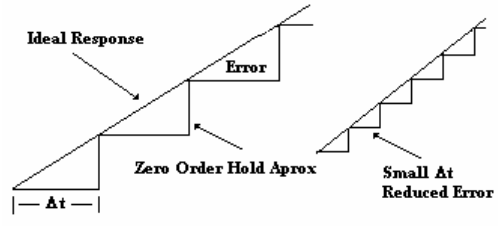


Figure 14: (a) Zero order hold approximation with large Δt, (b) smaller Δt smaller Error

IV STABILITY BOUNDARIES OF THE CP-PLL

In this section the stability boundary of the proposed model is compared to that of Gardner's model [1] for the second order DPLL, and a simulink model of the DPLL. The stability boundaries of the proposed technique are determined here for a pull in rate of 1%, 20% and 40% and are shown in Figure 15 along with Gardner's boundary and the simulink defined boundary. The pull in rate can be determined from Figure 9 and is calculated as $100(\Delta_1+\Delta_2)/\Delta_1$.

It is clear from Figure 15 that the simulink model of the 'real' DPLL system suggests that Gardner's stability prediction is not conservative enough. In fact there is a significant region of contradiction between the two models where Gardner predicts stability and the simulink model predicts instability. The simulink model also verifies that the proposed technique is more accurate, producing more conservative results then Gardner, that are inside the stability region of the 'real' DPLL system.

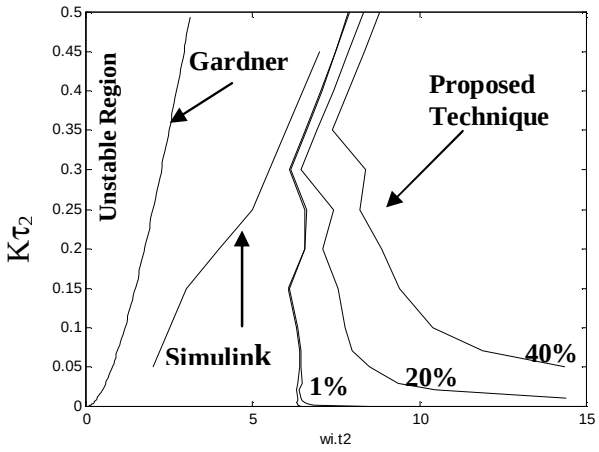


Figure 15: Stability boundaries of 1GHz second order PLL according to Gardner and the proposed piecewise linear model.

The second order CP-PLL creates a frequency jitter on the output of the VCO due to voltage jumps across the resistor when the CP current changes from 0 amps to +/- I_p. This is inherent to the second order system and is generally overcome by placing an additional capacitor in the loop filter. This is defined as C_3 in figure 4 and increases the order of the PLL to third.

In Figure 16, the stability boundaries for the 3rd order system are again compared for various values of b, where $b = 1+C_2/C_3$. The definition of b is not unique to this paper, it is similarly defined in [1].

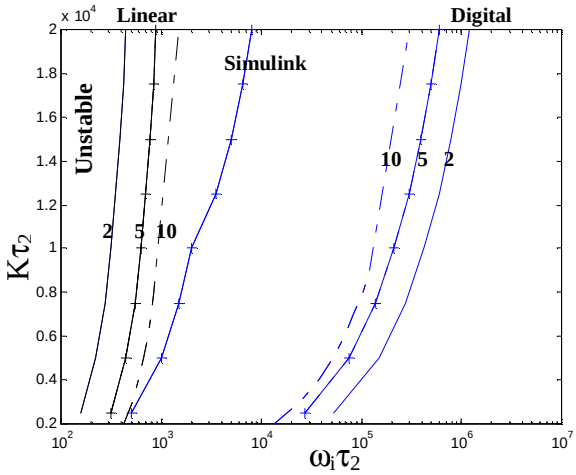


Figure 16: Third order Stability Boundaries

It is clear from Figure 16 above that similar to the second order system the proposed technique provides a much better prediction of the 'real' stability boundary.

V CONCLUSION

Traditional CP-PLL design techniques use linear theory and empirical methods to identify and design stable systems. It is shown in this paper that stability boundaries defined using traditional linear methods are too progressive, and actually identify regions as stable that are shown to be unstable when applied to a real CP-PLL system. The proposed technique uses piecewise linear methods to identify more conservative estimates of the stability boundary.

Two important properties of the proposed technique are also proven. Firstly, that the stability boundary is independent of any initial control voltage offset. However to avoid cycle slips, that would invalidate this technique, and increase the accuracy a small initial control voltage is suggested. Secondly, the state space curves of the CP-PLL converge into the equilibrium uniformly and do not intersect. The above two properties ensures that if one arc in state space of a particular system is determined, this will give an accurate representation of the response of this system regardless of the initial offset or subsequent path through state space.

Finally the proposed method is used to identify 2nd, and 3rd order stability boundaries and these are favourably compared to traditionally defined boundaries.

VI ACKNOWLEDGMENT

The authors acknowledge the support of the Enterprise Ireland Research Innovation fund grant.

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