National Semiconductor

Description of Boundary-Scan

Boundary-Scan Circuitry

The scan cells used in the Boundary-Scan register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals see *Figure 1.* AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

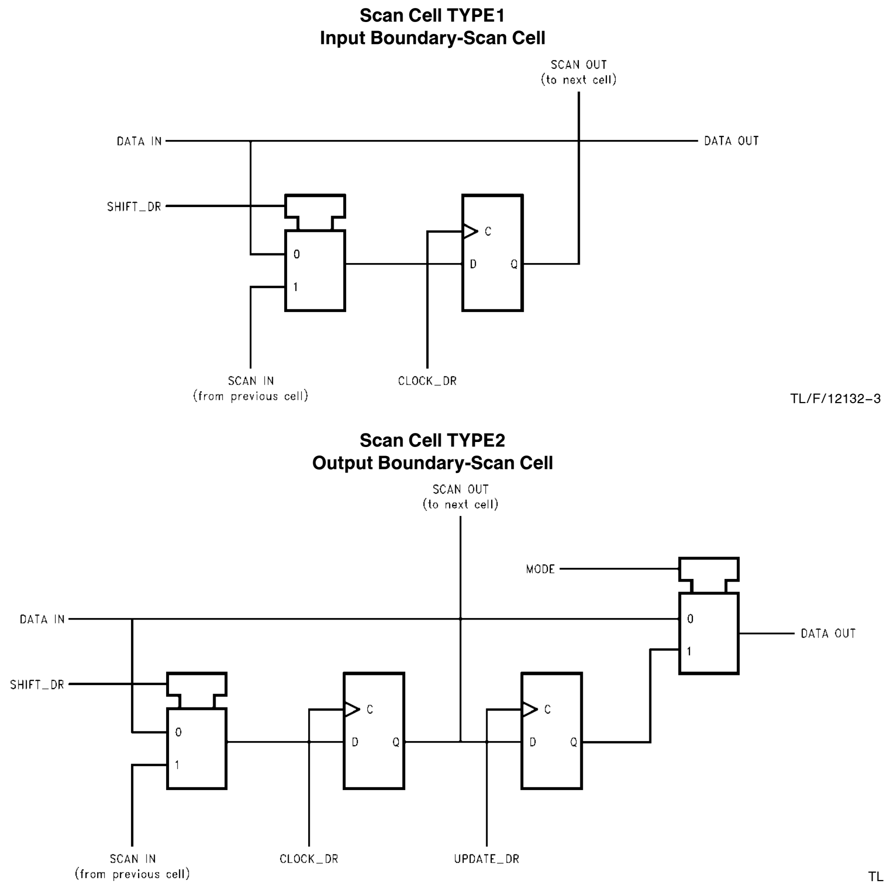

FIGURE 1. Type 1 and Type 2 Scan Cells are Located at Input and Output Pin, Respectively

Boundary-Scan Registers

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

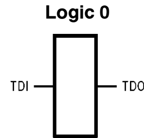

FIGURE 2. Bypass Register Scan Chain Definition

TABLE Ia. Scan ABT Product IDCODE (32-Bit Code per IEEE 1149.1)

Device	Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
SCAN182245A	0000	111111	0000000000	00000001111	1
SCAN182373A	0000	111111	0000001000	00000001111	1
SCAN182374A	0000	111111	0000000111	00000001111	1
SCAN182541A	0000	111111	0000001001	00000001111	1

MSB **LSB**

TABLE Ib. SCAN CMOS Device Identification (8-Bit Code Described in Device BSDL)

Device	8-Bit Code
SCAN18245T	00111101
SCAN18373T	00101101
SCAN18374T	00011101
SCAN18540T	01001101
SCAN18541T	10111101

Scan ABT devices include the 32-bit 1149.1-compliant IDCODE as shown in Table Ia. Scan CMOS devices do not include the IDCODE, however they do have an 8-bit device identification code which is described in its device BSDL model and shown in Table Ib.

Tables IIa, IIb and IV show which instructions are included for SCAN ABT and SCAN CMOS.

The INSTRUCTION register *Figure 3* is an 8-bit register which, for SCAN ABT, captures the default value of 10000001 (SAMPLE/PRELOAD, Table IIa) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is not required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction.

In the case of SCAN CMOS, the 8-bit INSTRUCTION register captures the device's 8-bit identification code in Table Ib. For more information refer to the section on instruction definitions.

TABLE IIa. SCAN ABT Instruction Registers

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

TABLE IIb. SCAN CMOS Instruction Register

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All Others	BYPASS

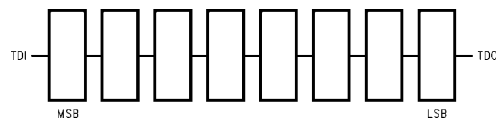

FIGURE 3. Instruction Register Scan Chain Definition

Boundary Scan Overview

This document is a supplement to the National Semiconductor SCAN Test Access Logic products datasheets. It provides an overview of the IEEE 1149.1 (boundary scan) circuit features included on the National's SCAN devices. The IEEE 1149.1 Std. document should be consulted for more detailed information about the IEEE 1149.1 standard requirements.

The IEEE 1149.1 boundary scan standard circuitry is comprised of 3 functional blocks—a test access port (TAP), a TAP controller and a set of registers.

I. TEST ACCESS PORT (TAP)

The Test Access Port (TAP) consists of four pins dedicated solely to the operation of the test logic. The four pins include TMS (Test Mode Select), TDI (Test Data In), TDO (Test Data Out), and TCK (Test Clock). These products contain a power-up reset function in lieu of adding the $\overline{\text{TRST}}$ pin. The motivation of this option is to save package size and hence customer board space, thus making the decision to implement 1149.1 less costly to the system designer.

TCK: This input provides the test clock for the test logic defined by the IEEE 1149.1 Standard. In accordance with the standard requirements, all test logic will retain its state indefinitely upon stopping TCK at a logic low, or 0. Additionally, the same retention may occur upon stopping TCK at a logic high, or 1, which is a permission granted by the standard. The motivation for TCK to be a dedicated test input is 1) to insure that it can be used independently of system clocks running at different frequencies, 2) that it permits shifting of test data without altering any system logic state when undertaking on-line system monitoring tasks, and 3) that it can be used to test all board interconnect even when that interconnect transfers clock signals from one device to another.

TMS: This input is the command signal to control system operation modes. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. The requirement that an unforced TMS input produce a logic high is to ensure that the normal operation of the design can continue without interference from the test logic by guaranteeing that an undriven TMS input can put the TAP Controller into the Test Logic Reset state.

TDI: This signal provides the serial data input of test instructions and data to the test logic. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. Test data will arrive at TDO without inversion after the appropriate number of clock cycles as determined by the length of the register currently connected between TDI and TDO. The requirement that an unforced TDI input produce a logic high is to assist in the determination of manufacturing defects in the test scan chain interconnect. A consistent field of 1's in shifting out the data registers can indicate where a break in the scan chain interconnect occurred.

TDO: This signal provides the serial data output of test instructions and data from the test logic. Changes in the logic state and drive activity for this output occur upon the falling edge of TCK. This is to avoid a race condition when TDO is connected to TDI of the next chip in the scan chain which is sampled on the rising edge. This output shall remain inactive except when the scanning of data is in progress. This is to permit the ability to multiplex scan chains on the board without causing signal contention between multiple TDO outputs connected together to form parallel scan chains.

II. TAP CONTROLLER

The TAP controller is a 16 state finite state machine which controls the insertion of the data and instruction registers (described later in this document) between TDI and TDO pins, and controls the flow of data through these registers.

Changes in the state of the TAP Controller (see *Figure 4*) are solely a response to the value of TMS upon the rising edge of TCK, or upon power-up (or the application of a logic low to the optional $\overline{\text{TRST}}$ input which is not included in the products referring to this document). In any given state actions of the test logic taken in that state occur on the falling or rising edge of TCK following the rising edge of TCK which caused the TAP Controller to enter the state initially.

Note: It may happen that actions to occur in one state happen on the same rising edge of TCK that cause the TAP Controller to enter the next state.

Test Logic Reset: In this state, the boundary scan test logic is disabled to allow the device to function normally. All boundary scan registers are reset to their default states. This state is entered by at most, five TCK cycles while holding TMS high or asynchronously by pulling TRST low (if TRST pin is included). The IEEE 1149.1 standard requires that an internal pull-up be included on the TMS pin to assure the TAP will return and remain in test logic reset if TMS is floating.

Run Test/Idle: This state provides a dual purpose depending on the active instruction. It is included to allow for optional or user defined tests, including BIST, to be performed. For the required IEEE 1149.1 instructions, all test data registers retain their current state (i.e., remain idle).

SELECT-DR Scan: This is a temporary state in which all test data registers retain their previous values.

Capture-DR: In this controller state data may be parallel loaded into the data register selected by the current instruction; otherwise, it retains its previous values.

SHIFT-DR: In this state the test data register selected between TDI and TDO by the current instruction will shift one stage at each rising edge of TCK. TDO is active during this state. Test data registers not selected by the current instruction maintain their previous values.

Exit1-DR: This is a temporary state in which all test data registers retain their previous values.

PAUSE-DR: This is a temporary state in which all data registers retain their previous values. This state is intended to temporarily halt the shifting of test data into the data register selected while retaining the ability to keep TCK running; TCK may be a free-running clock. This state is often used to load additional test vectors from external memory.

Exit2-DR: This is a temporary state in which all test data registers retain their previous values.

UPDATE-DR: The parallel output register of the selected test data register may be updated on the falling edge of TCK in this state, provided the test data register has such a parallel output register. The intent of the parallel output register is to provide the ability to apply the contents of the test data registers to the test logic simultaneously rather than applying it as it is being shifted in. All test data registers not selected by the current instruction retain their previous values.

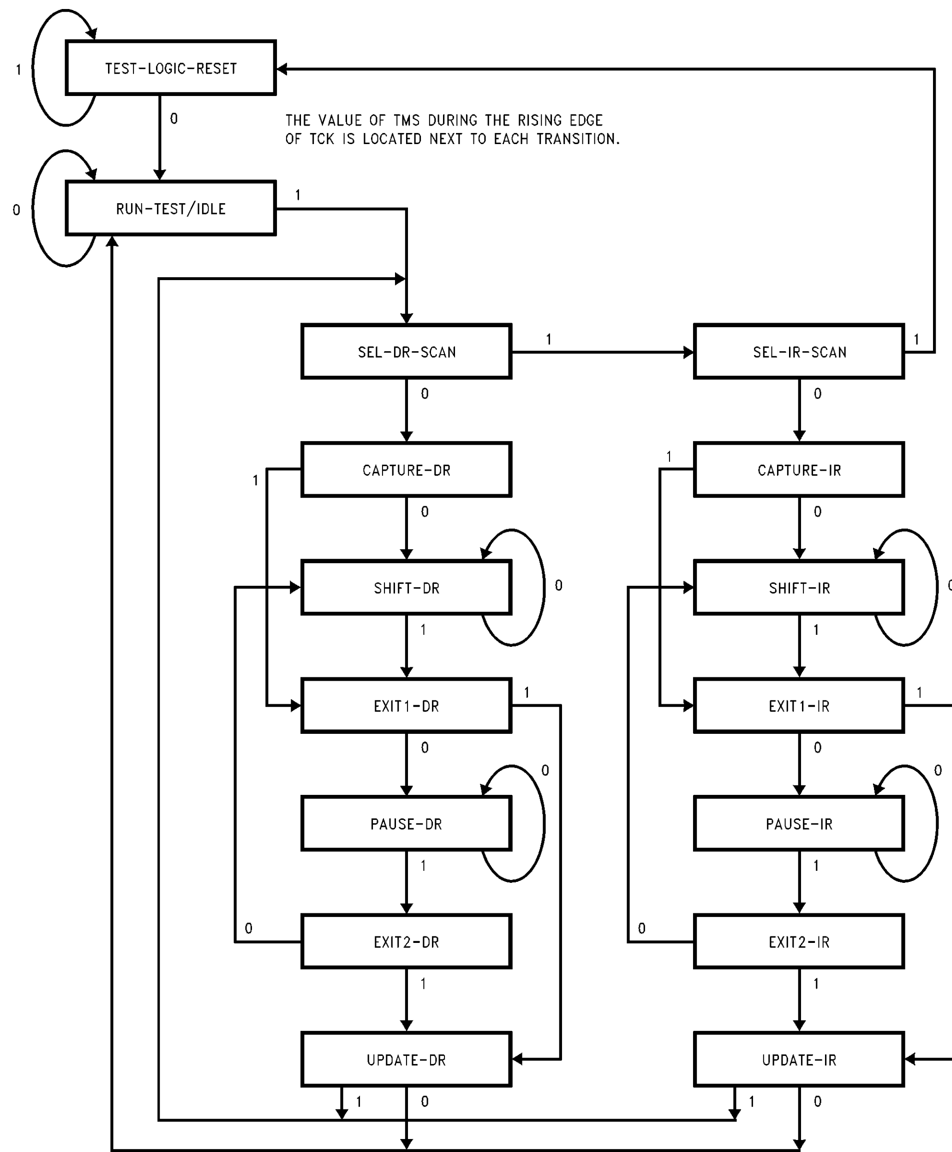

FIGURE 4. TAP Controller State Diagram

SELECT-IR Scan: This is a temporary state in which the INSTRUCTION register retains its previous value.

Capture-IR: In this controller state, a fixed value must be parallel loaded into the INSTRUCTION register. The only restriction on what that data may be is that its least significant bit must be a logic high, or 1, and its second least significant bit must be a logic low, or 0. These opposite state bits can be used to check the correct operation of the scan chain on the board by forcing a bit toggle when the instructions are shifted.

SHIFT-IR: In this state the INSTRUCTION register selected between TDI and TDO will shift one stage at each rising edge of TCK. TDO is active during this state.

Exit1-IR: This is a temporary state in which the INSTRUCTION register retains its previous value.

PAUSE-IR: This is a temporary state in which the INSTRUCTION register retains its previous value. This state is intended to temporarily halt the shifting of test data into the INSTRUCTION register while retaining the ability to keep TCK running. This state is often used to load additional test vectors from external memory.

Exit2-IR: This is a temporary state in which the INSTRUCTION register retains its previous value.

UPDATE-IR: The parallel output register of the INSTRUCTION register will be updated on the falling edge of TCK in this state. The intent of the parallel output register is to provide the ability to apply the contents of the INSTRUCTION register to the test logic simultaneously rather than applying it as it is being shifted in.

TDO OUTPUT ACTIVITY

Control of the TDO output buffer follows Table III.

TABLE III. TDO Output Buffer Control

Controller State	Register Selected between TDI and TDO	TDO Driver
Test Logic Reset	BYPASS	Inactive
Run Test/Idle	BYPASS	Inactive
SELECT-DR Scan	**	Inactive
SELECT-IR Scan	INSTRUCTION	Inactive
Capture-IR	INSTRUCTION	Inactive
SHIFT-IR	INSTRUCTION	ACTIVE
Exit1-IR	INSTRUCTION	Inactive
PAUSE-IR	INSTRUCTION	Inactive
Exit2-IR	INSTRUCTION	Inactive
UPDATE-IR	INSTRUCTION	Inactive
Capture-DR	**	Inactive
SHIFT-DR	TEST DATA	ACTIVE
Exit1-DR	**	Inactive
PAUSE-DR	**	Inactive
Exit2-DR	**	Inactive
UPDATE-DR	**	Inactive

Note: ** = Data register selected depends on currently active instruction.

FEATURES OF THE TAP CONTROLLER

The TAP Controller will not be initialized by the operation of any system pin such as a system reset. The TAP Controller will be initialized into the Test Logic Reset state upon power-up. This requirement is intended to avoid bus signal contention upon system power-up by disabling the test logic which allows the system logic to operate normally and hence be controlled to avoid any contention. (The TAP Controller will return to the Test Logic Reset state after, at most, five clock cycles of TCK with TMS high; but the time required to enact that operation may not be sufficient to avoid contention.)

Note that the TAP Controller has been defined such that six of the sixteen states have the ability to maintain their state provided that TMS remains at the same value it had when entering the state. Those states include Test Logic Reset to hold off the test logic during normal system operation, Run Test/Idle to undertake multi-cycle self tests, SHIFT-DR and SHIFT-IR to maintain the data shifting process for an extended period, and PAUSE-DR and PAUSE-IR to halt the shifting process while some other activity is performed such as retrieving test data from additional memory. This feature is available in any/all states where multiple clock cycles may be required to achieve the desired outcome or where activity is to be halted but still provide the ability to make TCK a free-running clock.

III. BOUNDARY SCAN REGISTERS

INSTRUCTION REGISTER

The INSTRUCTION register permits specific commands to be shifted into the design to select a particular test data register and/or a specific test function. Additionally, the capture sequence of the INSTRUCTION register permits design specific data to be examined.

The INSTRUCTION register must be at least two bits long, the specific INSTRUCTION register included into the devices which reference this document is eight bits long, and the two least significant bits must capture the value ‘‘01’’. The significance of the two bit minimum length is two fold. First it permits the ability to supply unique codes for at least each of the three mandatory instructions required by the standard. Secondly, the bit value ‘‘01’’ in the least significant locations can be used to check the connectivity of the scan chain by forcing a bit toggle at each instruction during a scan of the INSTRUCTION registers. This technique not only assists in determining the correct connectivity of the scan chain about the board, but also assists in pin-pointing the location of any break in the scan chain.

All of National’s SCAN Test Access Logic devices utilize an 8-bit instruction register. For the SCAN CMOS Test Access Logic devices, the 6 most significant bits which are loaded into the instruction register during the CAPTURE-IR state are used to provide a ‘‘pseudo ID code’’. The different codes captured into the INSTRUCTION register is a means of distinguishing the products in order to supply a method of evaluating the correct board placement of the products when an interrogation is performed through the scan chain only.

The captured ‘‘pseudo ID code’’ value is provided in each of the SCAN CMOS Test Access logic datasheets.

The SCAN ABT Test Access Logic devices include the IEEE 1149.1 optional ID CODE register and each device captures the same fixed value. This fixed value is the opcode for the SAMPLE/PRELOAD instruction, 1000001.

The order of scan through the INSTRUCTION register must be least-to-most; that is, the least significant bit is closest to TDO for a loaded instruction. During the SHIFT-IR state the instruction shifts one bit between TDI and TDO upon each rising edge of TCK and appears without inversion at TDO following the appropriate number of TCK cycles depending

on the fixed length of the INSTRUCTION register. A latched parallel output register accompanies each bit of the INSTRUCTION register such that the instruction can be updated or applied to the test logic simultaneously, rather than during the shift sequence. This latched parallel output changes upon the falling edge of TCK in the Update-IR state as well as upon the falling edge of TCK during the Test Logic Reset state. (It changes asynchronously upon the low assertion of the $\overline{TRST}$ input or upon power-up.)

Each instruction will identify a particular test data register to be connected between TDI and TDO when in the Shift-DR state along with defining any particular test actions to occur to that test data register and/or any others.

INSTRUCTION DEFINITIONS

The required instructions (see Table IV) include the BYPASS, EXTEST, and SAMPLE/PRELOAD instructions with optional instructions of HIGH-Z and CLAMP; and, for SCAN ABT only, the IDCODE. The additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT have also been incorporated into the SCAN ABT devices. The optional INTEST instruction was not incorporated because it adds a delay penalty to the system logic from gating that logic in order to provide controllability as well as observability. In the following descriptions each instruction will identify the test data register to be connected between TDI and TDO during the SHIFT-DR state, any restrictions on the binary codes used to implement the instruction, and what test data registers are used in undertaking the actions of the instruction.

1. **EXTEST.** This instruction allows circuitry external to the component package, typically the board interconnect, to be tested. Boundary-Scan register cells at the output pins are used to apply test stimuli, while those at the input pins capture test results. When this instruction is selected, the states of all signals on the system input pins will be loaded into the Boundary-Scan register upon the rising edge of TCK in the Capture-DR state and the contents of the Boundary-Scan register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-DR state. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 000. . .0 instruction binary code must invoke the EXTEST instruction. During this instruction the Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state. Additional binary codes for this instruction are permitted.

2. **SAMPLE/PRELOAD.** This instruction allows a "snapshot" of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan SHIFT register prior to selection of another Boundary-Scan test instruction. During this instruction the Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state. When this instruction is selected, the states of all signals on the system pins will be loaded into the Boundary-Scan register upon the rising edge of TCK in the CAPTURE-DR state and the contents of the Boundary-Scan register will be loaded into the parallel output register included with the Boundary-Scan register bits upon the falling edge of TCK in the UPDATE-DR state.

   Note that by interfacing these two actions through the Exit1-DR state, the current state of the system pins can be captured into the Boundary-Scan register and stored into its parallel output registers for later application back onto those same pins. When the SAMPLE/PRELOAD instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. This instruction is mandatory under the guidelines of IEEE Standard 1149.1, but the binary code may be device specific.

3. **BYPASS.** This instruction allows rapid movement of test data to and from other components on a board that are required to perform test operations by selecting the BYPASS register, a single-bit shift-register stage, between TDI and TDO in the SHIFT-DR state to provide a minimum-length serial scan path. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 111. . .1 instruction binary code must invoke the BYPASS instruction. This specific opcode, along with the requirement that an undriven TDI input produce a logic high value, is intended to load the BYPASS instruction during an instruction-scan cycle if the scan chain is broken. In such a case all instructions following the break in the scan chain will be loaded with the BYPASS instruction and hence have no impact upon the system's normal functional operation. Additional binary codes for this instruction are permitted. When the BYPASS instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. When the optional IDCODE register is not included, this instruction is loaded into the INSTRUCTION register in the Test Logic Reset state.

TABLE IV. Required and Optional Instructions Included

IEEE 1149.1	SCAN ABT	SCAN CMOS
Required	BYPASS	BYPASS
Required	EXTEST	EXTEST
Required	SAMPLE/PRELOAD	SAMPLE/PRELOAD
Optional	HIGH-Z	HIGH-Z
Optional	CLAMP	CLAMP
Optional	IDCODE	
Optional	SAMPLE-IN	
Optional	SAMPLE-OUT	
Optional	EXTEST-OUT	

4. **CLAMP.** This instruction allows fixed guarding values to be placed on signals that control the operation of logic not involved in the test, but does not require that the Boundary-Scan register be part of the serial scan path as in the EXTEST instruction. The contents of the Boundary-Scan register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-IR state for this instruction. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.
5. **HIGH-Z.** This instruction allows all of a components system outputs to be placed in an inactive drive state to permit its outputs to be safely backdriven during testing of other integrated circuits on the printed circuit board. All outputs of the device will become inactive even if during their normal system function they are two-state outputs. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.
6. **IDCODE.** (SCAN ABT and PSC110F only.) This instruction allows a blind interrogation of an identification code that is unique to this device type. During this instruction the IDCODE Register is connected between TDI and TDO in the SHIFT-DR state.
7. **SAMPLE-IN.** (SCAN ABT only.) This instruction is analogous to SAMPLE/PRELOAD but shortens the SCAN chain to include only the input and control pin cells (see Input Boundary-Scan register definition diagram in each datasheet). During this instruction only the Input Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.
8. **SAMPLE-OUT.** (SCAN ABT only.) This instruction is analogous to SAMPLE/PRELOAD but shortens the SCAN chain to include only the output and internal TRI-STATE control cells (see Output Boundary-Scan register definition diagram in each datasheet). During this instruction only the Output Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.
9. **EXTEST-OUT.** (SCAN ABT only.) This instruction is analogous to EXTEST but shortens the SCAN chain to include only the output and internal TRI-STATE control cells (see Output Boundary-Scan register definition diagram in each datasheet). During this instruction only the Output Boundary-Scan register is connected between TDI and TDO in the SHIFT-DR state.

Each of the previously defined instructions fully indicates which data registers may operate or interact with the system logic while the instruction is current. Test data registers that are not selected by the current instruction must be controlled such that they do not interfere with the system logic or the operation of the test data registers currently selected. While a given instruction may lead to operation of more than one test data register, only one test data register may be connected between TDI and TDO during the SHIFT-DR state for the given instruction.

BOUNDARY-SCAN REGISTER

The Boundary-Scan register permits testing of printed circuit board interconnects such as opens and shorts while also providing access to the components inputs and outputs when testing or monitoring its system logic. This register, as with all test data registers included in a 1149.1-compliant device, must be of fixed length. Data applied at the TDI input must appear without inversion at TDO during the SHIFT-DR state following the appropriate number of TCK cycles determined by the specific fixed length. This test data register will shift one stage toward TDO at each rising edge of TCK in the SHIFT-DR state when selected by the current instruction. Data will be parallel loaded into the Boundary-Scan register upon a rising edge of TCK in the Capture-DR state and the parallel register stages of the Boundary-Scan register will be latched upon the falling edge of TCK in the UPDATE-DR state provided that it is selected by the current instruction; otherwise, no change to its contents shall occur.

The shift register stages used in the make-up of the Boundary-Scan register may or may not be required to incorporate a parallel output register as well as its shift register stage. This requirement depends on the function of the system logic pin with which it is associated as well as the operational requirements of that pin during certain instructions defined for the device. The Input and Output Boundary-Scan cells demonstrate the parallel register stage, or lack thereof. The first cell can be used on system input pins where only observability of its logic state is necessary while the second scan cell can be used at system outputs where observability and controllability are required. Note that in the input scan cell there is no multiplexer directly in the data path while one does exist in the output scan cell. It is the logic gating of the data path that results in the performance penalty of the data path when controlling test logic is added. It is for this reason that the optional INTEST instruction was not included as one of the available features on the products which specifically reference this document. It was deemed unnecessary to pay the performance cost in exchange for the limited functional extension of controlling inputs as well.

If INTEST capability is desired, the system logic of the products referencing this document can be considered an extension of the EXTEST capability. All 1149.1-compliant devices require that the input and output data path scan cells be placed at logically equivalent locations to the system pin. As a result of that action the input/output buffers and voltage level translators are already tested as an extension of interconnect tests. If these interconnect tests are combined with the triggering of a 374 flip-flop clock input, as an example, the internal logic of the device can be evaluated as an extension of the EXTEST capability. Because the National SCAN products currently offered have easily manipulated

system logic, the 1149.1 user can logically extend the internal system logic to the EXTEST function. This feature is available during the EXTEST instructions for these products because the state of the outputs is captured along with the state of the inputs during the rising edge of TCK in the CAPTURE-DR state. Note that this is contrary to a recommendation of capturing fixed values on the outputs during EXTEST, but it provides for a feature that would otherwise not exist.

While these cells are sufficient to observe the logic state of the signal in which they are placed, they have a limitation in observing the activity of such a signal as in the specific case of a three-stated output. To determine the activity as well as the logic state of such an output, two such scan cells are required. One in the data signal path and another in the output enable signal path. By observing at both locations the drive activity and/or logic value can be inferred. In thecase of a single output enable signal controlling more than one output data path, the output enable signal may be observable and controllable at a single location rather than at each specific output without loss of functional intent provided that the specific location retain control over all the data outputs in unison. This provision is included to reduce the hardware overhead as in the case of a device where such output enable signals are organized byte-wide.

The order of the required scan cells in the Boundary-Scan register is undefined by the 1149.1 Standard and hence can be device specific even if the system function of that device be identical to another 1149.1-compliant device. In other words, even if two identical system function devices are 1149.1-compliant there is no guarantee that such devices will be identical in the structure of the Boundary-Scan register.

A description of the Boundary Scan Register for each device is included in its datasheet.

Input Boundary-Scan Register (SCAN ABT only)

The Input Boundary-Scan register operates in a manner analogous to the full length Boundary-Scan register.

Output Boundary-Scan register (SCAN ABT only)

The Output Boundary-Scan register operates in a manner analogous to the full length Boundary-Scan register.

Please refer to the device datasheet for a description of its input and output Boundary-Scan Registers.

BYPASS REGISTER

The BYPASS register is also a test data register and therefore must comply with the definitions surrounding test data register operation; but its advantage is in its size, not necessarily in its function. The BYPASS register consists of a single shift register stage in order to shorten the board-level serial scan chain by bypassing some devices while accessing others. This feature is intended to reduce the software overhead in applying and retrieving serial test data by permitting a shortcut between TDI and TDO of any given integrated circuit in order to expedite access to others.

The BYPASS register must capture a logic low value upon the rising edge of TCK in the SHIFT-DR state provided that it is selected by the current instruction. This feature is designed to accompany those devices which incorporate the 32-bit device identification register. (The BYPASS register is a test data register whose least significant bit is a fixed logic high.) Upon an initial scan of the data registers connected across the board, all devices will either connect the BYPASS register or the optional device IDENTIFICATION register in its test data register scan path between TDI and TDO while in the SHIFT-DR state. (This condition is a result of power-up or a logic low assertion to $\overline{\text{TRST}}$ to initialize each 1149.1 device on board.) By shifting the data registers the retrieval of each logic zero indicates a BYPASS register connection until the first logic high is read. The logic high will be the framing bit of a device IDENTIFICATION register which would then indicate that the following thirty-one bits are identifiers to the specific device at that location of the scan chain. The requirement that the BYPASS register capture a logic low value is intended to form the background for the device IDENTIFICATION register framing bit. Additionally, the logic low value is opposite the value to be produced in the case of an undriven TDI input pin.

Device Identification Register

The device identification register is a 32-bit, read only register compliant with IEEE Std. 1149.1. When the IDCODE instruction is active, the identification register is loaded with a fixed, unique value upon leaving the Capture-DR state. The ID code register contains information pertaining to the device manufacturer, part number and revision. It is used to ensure the correct device is properly placed in the correct location within a boundary scan chain.

An identification (ID) register is included within the National SCAN ABT Test Access Logic devices. The specific ID register value is provided in the associated device datasheets.