Accurate simulation of switched systems using PSpice and VHDL-AMS

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INTRODUCTION

The paper deals with behavioral modeling of idealized systems with discontinuities. The purpose of such models is to obtain the first-order effects to verify analytic calculations or to increase simulation speed.

Traditional algorithms for the time-domain analysis implemented in Spice-class simulators are based on the assumption of smoothness and continuity. Abrupt changes of system parameters or even discontinuity during switching cause numerical errors. The VHDL-AMS language brings radically different approach in comparison with Spice [VHD99]. The system of differential algebraic equations (DAE) can be formulated explicitly and can be structurally changed during simulation. The basic principles will be demonstrated on the modeling of switched power supplies.

Numerical algorithms for the time-domain analysis of continuous-time circuits are based on the formulation of circuit equations into the DAE system

$$F(\dot{\mathbf{x}}, \mathbf{x}, t) = \mathbf{0} \ , \tag{1}$$

where $\mathbf{x}$ is the vector of unknowns. System (1) cannot be solved directly, but its solution $\mathbf{x}(t)$ is approximated by a discrete sequence $\mathbf{x}_n \approx \mathbf{x}(t_n)$. To find the (n+1)*th* step the adjoint algebraic system

$$G(\mathbf{x}_{n+1}, t_{n+1}, \mathbf{X}_n) = \mathbf{0} \tag{2}$$

should be solved. $\mathbf{X}_n$ is the matrix of past solutions up to $\mathbf{x}_n$. Various discretization methods are discussed in [Kun95]. System (2) is solved using the Newton-Raphson iteration method.

The time step $h_n = t_n - t_{n-1}$ is automatically adjusted according to the estimation of Local Truncation Error (LTE), which is inversely proportional to h [Kun95]. The minimum timestep is usually limited to

$$h \geq T_{final} \frac{10^{-n}}{RELTOL} \ , \tag{3}$$

where n is the precision of time representation in simulator, T_{final} is the length of simulation interval and $RELTOL$ is the simulator parameter. The lower limit is necessary to maintain the numerical precision of $t_{n+1} = t_n + h_{n+1}$ assignment.

The traditional Spice simulators require smooth solution of (1), VHDL expects piecewise smooth solution with a finite number of discontinuities where

$$\dot{\mathbf{x}}(t_n^-) \neq \dot{\mathbf{x}}(t_n^+) \text{ or even } \mathbf{x}(t_n^-) \neq \mathbf{x}(t_n^+) \ . \tag{4}$$

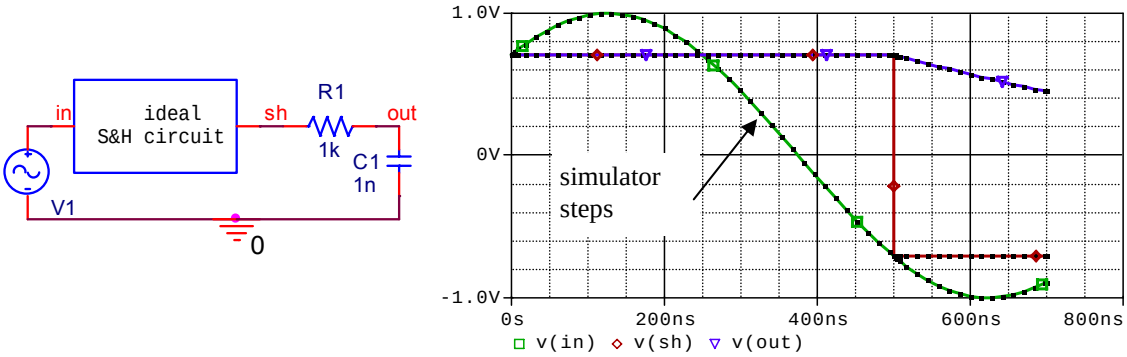
The discontinuity (4) can be handled easily by computing the solution at t_n^-, changing the system (1) and its state variables, and restarting the solution from t_n^+ using $\mathbf{x}(t_n^+)$ as the initial condition. The exact time t_n should be signaled to the solver explicitly.

Without the explicit signaling the simulator jumps over the exact time instant t_n in case when the LTE is acceptable or ends up with a “Timestep too small” message if limit (3) is reached. It should be noted that system (2) is still expected to be smooth in the neighborhood of $\mathbf{x}_{n+1}$.

New behavioral functions in PSpice

Starting with version 10.5 new functions for behavioral modeling, that make available the process of integration of (1), were implemented in PSpice. Function *break* allows scheduling a simulator step at the specified time, and functions *state* and *delta* make available the last three steps of selected node voltage.

Fig. 1 shows an example of behavioral model of simple sample&hold circuit with RC load. The sampling period is exactly 0.5μs. Two *break* statements are used to schedule each sampling event. Formally, the statements should be included as a definition of a dummy source. The upper limit for timestep was not set.

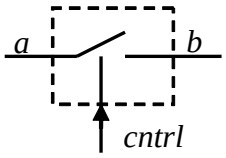



```
* signal source with dummy load
V1  IN 0 SIN 0 1 1meg 0 0 45 ;A=1V, f=1MHz, =45
Rdummy IN 0 1k
* ideal sampler with load
E1  SH 0 VALUE={if(intq(time/0.5u)==1,v(in),state(0,v(sh)))}
R1  SH OUT 1k
C1  OUT 0  1n
* breakpoint "schedulers"
Gbreak1  0 0 VALUE {break(ceil(time/0.5u)*0.5u)}
Gbreak2  0 0 VALUE {break(ceil(time/0.5u)*0.5u-1p)}
```

Figure 1 Ideal S&H circuit

Switched circuit modeling with VHDL-AMS

A switched system contains active and passive switches. Fig. 2 shows a VHDL-AMS model of an active (controlled) switch. The switch-on resistance R_A is allowed to be zero.




```
entity swq is
   generic (
    Ra : resistance := 0.0);
  port (
    terminal a,b: electrical;
    signal cntrl: in std_logic);
end entity swq;
```

```
architecture ideal of swq is
  quantity v across i through a to b;
begin
  if cntrl='1' use
    v == i * Ra;
  else
    i == 0.0;
  end use;
  break on cntrl;
end architecture ideal;
```

Figure 2 Model of ideal active switch

Discrete signal *cntrl* controls the behavior of the switch through the *if-else* statement in a piecewise manner. During iterations to obtain the solution of (2) for a particular time instant the value of *cntrl* does not change. Thus (2) is **continuous**. The *if* statement selects **which equation** will be used for the DAE system.

The exact time instant of changing the switch state should be signaled to the analog solver or else it “jumps over” the event. This is done by the *break* statement, Fig. 3.

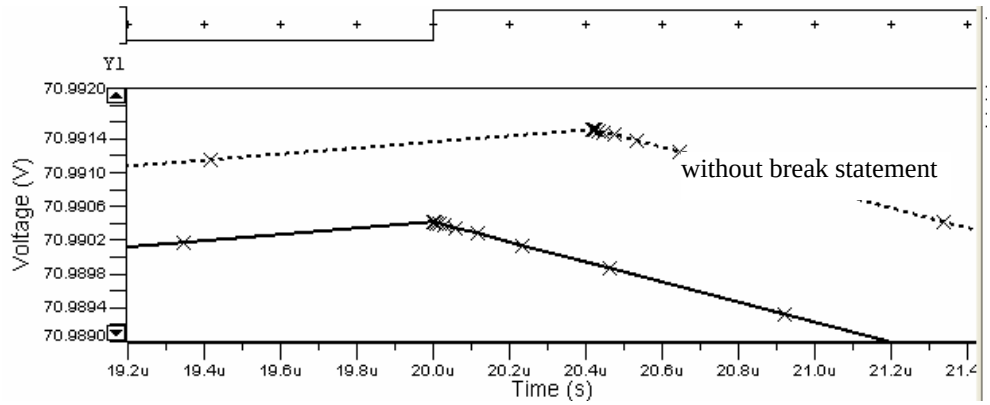
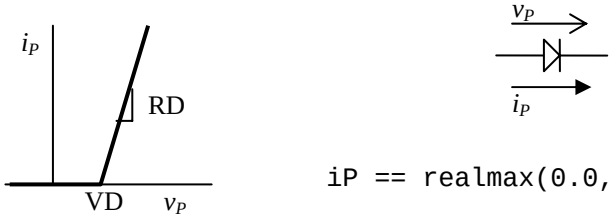


Figure 3 Effect of break statement (capacitor voltage from Fig. 5a)

The passive switch (diode) can be approximated by a piecewise linear function. Fig. 4 shows the approximation and a fragment of the VHDL-AMS code. This function introduces an *implicit* discontinuity that occurs during iterations of the analog solver. The effect is a numerical error similar to that in Spice simulators.




```
iP == realmax(0.0,(vP-VD)/RD);
```

Figure 4 Piecewise linear passive switch

A discrete signal *domain* whose value depends on the type of analysis is predefined in VHDL-AMS. With the *if* statement it is possible to select which equation to use for a particular analysis. This technique will be demonstrated on the time domain model of boost converter with accelerated finding of the steady-state solution.

The direct time-domain analysis of switched power supplies in the Spice and the VHDL-AMS simulators results in very long simulation times as the integration step depends on switching transients and the time interval of interest is usually several orders of magnitude longer. Since the steady-state analysis is not available in majority of simulators, the only possibility is to run a sufficiently long transient simulation.

The utilization of the averaged modeling technique results in an incomparably faster analysis [Dij95], [Bio06]. On the other hand, by smoothing the fast switching process we lose information about the output voltage ripple and other characteristics.

The steady-state solution of (1) is characterized by condition

$$\mathbf{x}(T) = \mathbf{x}(0) \ , \tag{5}$$

where T is the switching period. Finding the steady-state solution is equivalent to finding the appropriate initial conditions $\mathbf{x}(0)$. The utilization of the DC operating point as the initial condition, normally used for the transient analysis, is useless here.

The averaged model represents relations between short-time average values of all quantities. Finding a steady state-solution in the original model is equivalent to finding a DC operating point in the averaged model.

Fig. 5a shows a time-domain model of boost converter from [Dij95]. The following numerical values have been used:

V = 60V	Ro = 60Ω	C = 1000μF	L = 6mH
RL = 3Ω	T = 10μs	D = 0.25 (duty ratio)	
active switch:	RA = 1Ω (see Fig. 2)		
passive switch:	VD = 0.6V	RD = 1Ω (see Fig. 4)	

The technique of PWM switch has been used to obtain the averaged model [Dij95], [Bio06], Fig. 5b. It consists in the replacing both switches by two controlled sources. The model obtained is a linear circuit, which can be used for all basic analyses. It is valid from DC up to the Nyquist frequency ($f_{SW}/2$).

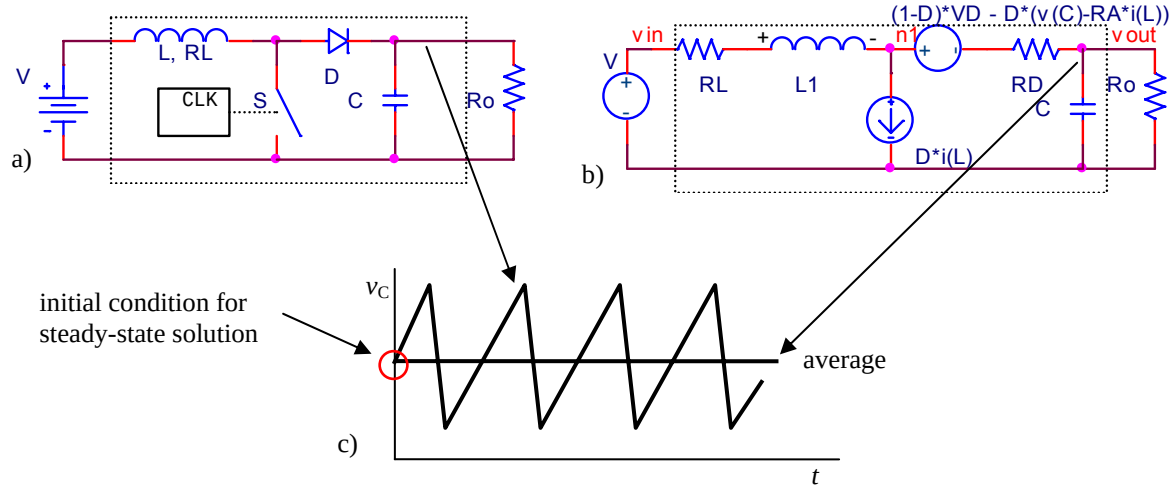


Figure 5 a) Boost converter; b) its averaged model; c) diagram of capacitor voltage

Fig. 6 shows the VHDL-AMS code of the behavioral model. For the DC and the AC domains the averaged model is used. The DC analysis corresponds to the steady-state analysis in the original circut. For the time domain the original model is used. If the DC (averaged) solution is used as the initial condition we obtain immediately the steady-state in the time domain. The first cycle of switching clock generator is shortened to correctly use the initial condition, Fig. 5c.

```
entity boost is
port (terminal vin, vout, vref:
      electrical;
  quantity D : in real);
end entity boost;

architecture md of boost is
  terminal n1  : electrical;
  signal   clk : bit := '0';
  quantity vL across iL through vin to n1;
  quantity vA across iA through n1 to vref;
  quantity vP across iP through n1 to vout;
  quantity vC across iC through vout to vref;
begin
--clock generator
Clock: process
begin
  clk <= '0';
  wait for Ts*(1.0-D)/2.0;
  loop
    clk <= '1';
    wait for Ts*D;
    clk <= '0';
    wait for Ts*(1.0-D);
  end loop;
end process Clock;
break on clk;
```

```
if domain = time_domain use
  --L, RL
  vL == RL*iL + L*iL'dot;
  --C
  iC == C * vC'dot;
  --active switch
  if clk='1' use
    vA  == iA * RA;
  else
    iA  == 0.0;
  end use;
  --passive switch
  iP == realmax(0.0,(vP-VD)/RD);
else
  -- other domains
  --L, RL
  vL == RL*iL + L*iL'dot;
  --C
  iC == C * vC'dot;
  --active switch
  iA  == D * iL;
  --passive switch
  vP == (1.0-D)*VD
        -D*(vC-RA*iL)+iP*RD;
end use;
end architecture md;
```

Figure 6 VHDL-AMS code of boost converter (definition of generic constants omitted)

Fig. 7 shows a comparison of the proposed steady-state analysis with a long transient simulation from zero initial condition. Even after 2000 switching periods the system still has not reached the steady-state.

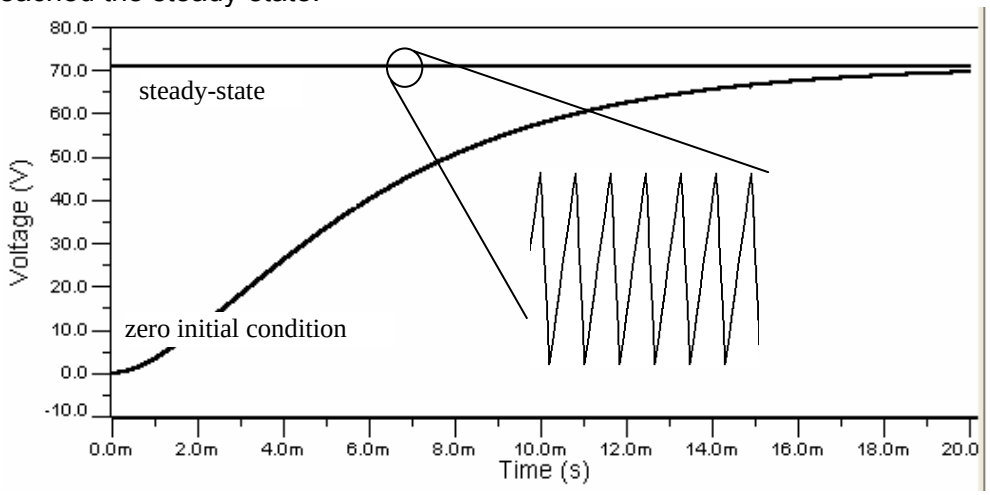


Figure 7 Comparison the zero initial condition with the averaged DC operating point

CONCLUSIONS

The modeling of idealized switched systems using the VHDL-AMS language has been shown. Although PSpice implements new functions for behavioral modeling the better tool is VHDL-AMS. The detailed analysis of circuits on the transistor level is still the domain of Spice simulators.

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