3rd International Conference on Electrical & Computer Engineering
ICECE 2004, 28-30 December 2004, Dhaka, Bangladesh

FAULT DETECTION AND DIAGNOSIS IN ANALOG INTEGRATED CIRCUITS USING ARTIFICIAL NEURAL NETWORK IN A PSEUDORANDOM TESTING SCHEME

Prithviraj Kabisatpathy[1], Alok Barua[2], and Satyabroto Sinha[2]

[1]Department of Information Technology, Biju Patnaik University of Technology, Bhubaneswar – 751003, Orissa, INDIA. E-mail: kabisatpathy@hotmail.com
[2]Department of Electrical Engineering, Indian Institute of Technology, Kharagpur – 721302, West Bengal, India, E-mail: alok@ee.iitkgp.ernet.in, ssinha@ee.iitkgp.ernet.in

ABSTRACT

The property of the Gaussian white noise that its auto-correlation is a single Dirac-δ function is exploited in this paper. The testing scheme proposed uses a pseudorandom noise as the input stimulus, thereby providing a good estimation of the impulse response of a circuit under test (assumed to be stable linear time-invariant circuit). The methodology is based on the use of model-based observer implemented through feed forward neural networks for fault detection and diagnosis in analogue integrated circuits. The methodology can be viewed as a built-in self-test along with a design for testability scheme that dramatically improves the fault coverage and can be implemented either on-line or off-line depending on the need of the application and silicon area overhead. Its main advantages are: a universal input stimulus (white noise) is used and thus test generation can be simplified, good and faulty signatures for high quality testing can be easily constructed and testing cost can be minimised.

1. INTRODUCTION

With growing complexity and shrinking device dimensions, integrated circuit (IC) performances are becoming increasingly sensitive to inherent fabrication parameter deviations. Consequently, testing has become one of the major cost factors in the over-all IC manufacturing costs. The motivation for test is to eliminate test escapes and reduce the number of good devices identified as faulty by the test program. Design for test (DFT) and built-in self-test (BIST) techniques for analogue and mixed signal circuits have recently attracted considerable interest for helping in reducing test related difficulties. For systems-on-chip there is an absolute need for BIST support to reduce test cost, improve test coverage and support testable designs. In the majority of cases, BIST is based on DFT optimizations at various levels. Many authors [1, 2] have discussed analog DFT solutions. Other interesting techniques like the pattern recognition capabilities of artificial neural networks (ANNs) to diagnose faults [3, 4], supply current monitoring for testing analog and mixed-signal circuits [5, 6], or analog and mixed-signal circuit testing by power supply voltage control [7]are attractive directions. The BIST techniques proposed in literature [8, 9] concern especially with on-line testing. However, due to their prohibitive silicon area overhead, these techniques are only viable for highly crucial applications. Slamani et al. [10] have discussed an off-line BIST technique.

We have chosen a diagnostic framework for the analog ICs using a pseudorandom noise generator as the test pattern generator and a model-based observer to detect and diagnose faults [11]. The observer is implemented through a multi-layer feed-forward ANN trained with back-error propagation (BEP) algorithm.

2. THE TESTING STRATEGY

A fault in an analog IC can be either catastrophic or parametric. In most cases, the former is caused by physical defects, which change the topology of the chip (e.g., the short/bridging faults) while the latter is caused by the variations in the device parameters. In general, the chip subject to the catastrophic faults will be completely out of function and therefore these faults can be easily detected. On the other hand, the chip subject to the parametric faults will still function but the performance is degraded.

There is a region of acceptable behaviour around nominal. Beyond this region, the performance does not meet design specification, but does not cause complete circuit failure. Finally there are faults that render the circuit inoperable. Therefore the taxonomy of analog faults can be represented as shown in Figure 1. So one must choose a subset of faults, which will lead to the best possible fault list.

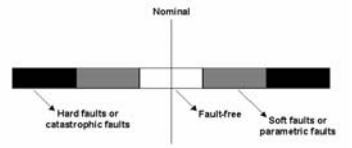

Fig. 1 Taxonomy of analog faults.

In this paper, we propose a fault-model-driven testing technique, which requires only a simple output response measurement. The basic approach of the diagnosis method is to compare the circuit under test against a mathematical model of the fault-free circuit, implemented using a simple multi-layer ANN trained with BEP algorithm. The strategy proposed is based on the excitation of the analog IC being tested with a pseudorandom noise (PRN) and subsequent measurement of the transient response at the output node(s). The consideration that the CUT may be driven outside its region of linear operation, for which it is to be tested, motivates the use of a wide spectrum noise with a constant magnitude over all the frequencies. Another advantage of the PRN is that it will allow diagnosis to be performed through the primary inputs and outputs of the CUT. This may reduce the amount of additional circuitry necessary when inserting control and observation points in the DFT structure of the circuit. Figure 2 shows the proposed system overview for fault diagnosis of analog integrated circuits using model-based fault detection and fault isolation [12, 13].

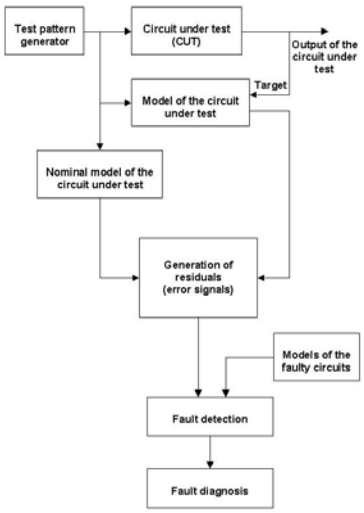

Fig. 2 An overview of the proposed testing strategy.

The procedure of the proposed model-based fault diagnosis in analog ICs can roughly, be divided in to the following three stages:

1. signature generation,
2. generation of the residuals (or fault signatures), and
3. detection and isolation of faults.

The first stage involves the definition of different fault classes. The circuit under test is simulated using the pseudo-random noise as the test stimulus for each fault class induced. The output response of the circuit under test forms the signature for that fault class.

For the residual generation three kinds of models are required: nominal, actual (observed) and that of the faulty circuit under test. For a realistic representation, it is important to model all effects that can lead to the detection of a fault, genuine or otherwise. All the models are created using simple multi-layer ANN consisting of one input layer, one or two hidden layers and one output layer. The ANN models are trained using BEP algorithm to output the CUT responses under fault-free and different fault conditions. The fault-free ANN model accommodating allowed component tolerances represent the nominal model. The difference between the outputs of the nominal model and the model of the actual CUT generates the desired residual. When there is no fault then the two models (the nominal and the actual) will present a very close behaviour resulting in a negligibly small residual. Under faulty condition the system will generate a residual showing how much the actual circuit is different from the fault-free circuit. Any fault in the circuit, be it catastrophic or parametric, will change the signature of the residual. These residual signatures of known fault conditions of the circuit, known as the fault signatures, are first simulated and stored in a model bank for future use.

The detection and isolation of faults involves modelling of the actual CUT to the application of the PRN, generating the residual and comparison of this residual to that of different fault signatures simulated and stored in the model bank. Depending on the specific application, the number of distinct fault signatures stored in the model bank can range from zero to hundreds. Making provisions for common fault signatures gives the advantage of a fast, predetermined response to such faults. It is interesting to notice that this explains the robustness of the methodology.

3. TEST RESULTS

In order to explain the proposed test methodology, we have chosen, as examples, the Fairchild μA741 Op-Amp, a single amplifier band-pass filter [3], the CMOS Op-Amp and the continuous time state variable filter from the IEEE Analog and Mixed-Signal Benchmark Circuits [14]. The Op-Amps are widely used as building block components for many analog designs and therefore the testability deserves thorough investigation.

3.1 Stand-alone Op-Amps

The Op-Amp is used in the voltage follower configuration. All the parameters were assigned ±5% statistical variations. The number of fault classes depends on the level of diagnosis desired. Go/no-go testing requires only two classes: faulty and fault-free. For complete component level diagnosis more number of fault classes is required. All faults may not be required to be simulated. Keeping this in mind catastrophic faults like various short circuits and open circuits and various parametric faults for the μA741 Op-Amp like forward and reverse β, junction capacitance, transport saturation current, forward Early voltage, forward and reverse transit time etc. and for the MOS Op-Amp channel length, channel width, saturation current, threshold voltage, oxide thickness, etc. were investigated. The nominal values of the BJT PSpice parameters of the μA741 Op-Amp were taken from Wooley et al. [15] and that of the CMOS Op-Amp were taken from the IEEE mixed-signal benchmark circuit homepage at: http://faculty.washington.edu/manisoma/madtest/benchmarks/ .

Both the Op-Amps were simulated in the voltage follower configuration using PSpice and Monte-Carlo techniques for fault-free and different faulty conditions using PRN as its input stimuli. Non-faulty components were allowed to vary within their specified tolerance range to establish the signature for fault-free CUT. The data obtained from these simulations was normalised and transferred to the MATLAB environment for use in the simulation of the ANN models and generation of the fault signatures using the neural network toolbox.

A small multi-layer ANN was used to model the fault-free as well as all the faulty classes. The ANN model generated for the nominal fault-free Op-Amp is designated as the nominal model of the CUT. The difference between the output of this nominal model when subjected to the PRN input and the output response of any other ANN model subjected to the same input gives an error signal, which is the residual. These error signals or residuals are stored as fault signatures in a model bank.

3.2 Embedded Op-Amps

For the purpose of testing the validity of the proposed methodology for embedded Op-Amps two examples were selected using μA741 Op-Amp. One was a single amplifier band-pass filter [3] and the other one was the continuous-time state variable filter [14]. The circuits were simulated using Pspice and Monte-Carlo techniques for fault-free as well as different faulty conditions using PRN as the input test stimuli. As previously stated, non-faulty components were allowed to vary within their specified tolerance range to establish the signature for fault-free circuit. The output response of the fault-free band-pass filter and that of the state variable filter circuits are shown in Figures 3 and 4 respectively.

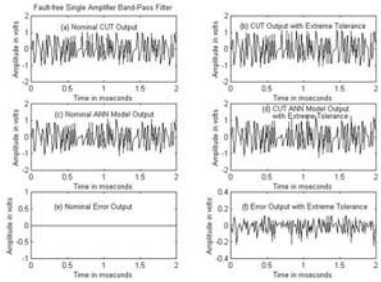

Fig. 3 Output response, the output of the ANN model and the error outputs of fault-free band-pass filter circuit.

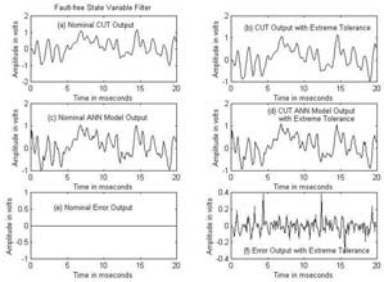

Fig. 4 Output response, the output of the ANN model and the error outputs of fault-free state variable filter circuit.

Once the DATA is obtained from the above simulation, a multi-layer ANN trained with BEP algorithm was used to model the fault-free as well as faulty circuits using the neural network toolbox. The network contains an input layer having 1 input neuron with the sigmoid threshold function, 2 hidden layers having 15 neurons each with the sigmoid threshold function, and an output layer having one output neuron with a linear threshold function. Now PRN is applied to these models and the output is compared to that of the nominal fault-free model with the same input to get the fault signatures. All these signatures obtained are stored in a model bank for reference during actual testing of the circuits. Once the fault signatures for known fault conditions are obtained and stored in the model bank, the diagnostic system is ready for use. Figures 3 and 4 also show the outputs of the nominal and fault-free ANN models and the nominal and maximum values of the fault-free signatures of the band-pass filter and the state variable filter respectively.

If a fault is detected at the time of the diagnosis of the circuit, the fault signature of the circuit under test is compared with the individual fault signatures stored in the model bank for classification of the fault.

Examples of output response, the output of the ANN model, the nominal and maximum fault signatures of faulty band-pass and state variable filter circuits are depicted in Figures 5 and 6 respectively. The result obtained by the authors in this simulation study is quite promising.

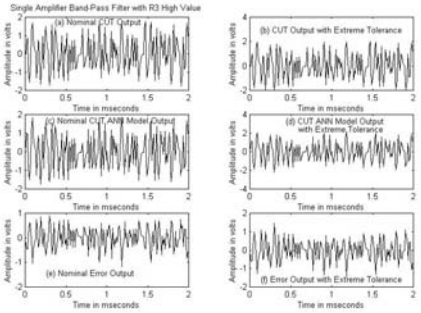

Fig. 5 Output response, the output of the ANN model and the error outputs of faulty band-pass filter circuit with resistance R3 high value.

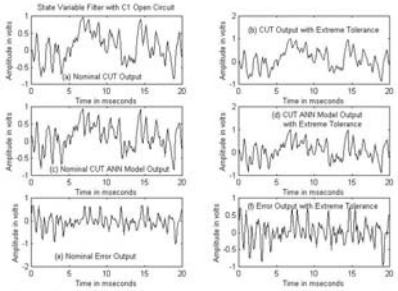

Fig. 6 Output response, the output of the ANN model and the error outputs of faulty state variable filter circuit with Capacitor C1 open circuit.

4. CONCLUSIONS

A simple fault diagnosis technique for analog ICs has been presented. Because the pseudorandom test stimulus provides a natural spread spectrum test signal, the test generation problem is completely eliminated and it can be used as a universal stimulus for testing of analog ICs, particularly for those, which are amenable to small signal operation at least under test conditions. The efficiency of the proposed testing strategy relies on the proper choice of signatures and discrimination schemes to distinguish between the fault-free circuit and the faulty circuit in the fault dictionary. The strategy is successfully tested to detect both hard and soft faults in Op-Amps and circuits using Op-Amps. The simulated experimental results obtained indicate that the proposed method of model-based observer using artificial neural networks is quite robust.

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