Parametric Fault Diagnosis for Analog Circuits Based on Neural Networks

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***Abstract* —This paper presents a parametric fault diagnosis approach for analog circuits based on Neural Networks. The major challenge in neural network based analog fault diagnosis is the high complexity of neural networks when the number of faults is large. Instead of designing and training a large complex neural network, we develop simple neural networks for each fault to enhance the efficiency. Sensitivity guided input selection [1] is used to reduce the number of measurements. Faults are injected at the process level while also taking process variations into account. Experiments on a two-stage amplifier circuit confirm the accuracy and efficiency of our method.**

I. Introduction

Fault diagnosis is an important technique in the circuit development stage. It has become an active research area since 1970's and various useful techniques have been suggested in literature, including the use of fault dictionaries, support vector machines, and neural networks [2, 3]. Even though much progress has been made in the digital domain, diagnosis for analog circuits still constitutes a major roadblock.

Analog fault diagnosis is challenging, due to the continuous behavior, increasing complexity, nonlinear effects, and increasing process variability. This difficulty in modeling makes neural networks an appealing tool to use in this area since they can compact the information in the form of a number of network parameters. In this sense, the network itself can work as a compact fault dictionary. The process of creating and verifying the fault dictionary are completed simultaneously, which significantly reduces computation time. Therefore, neural networks offer a very promising approach to fault diagnosis of analog circuits.

Most of prior approaches that use neural networks in analog fault diagnosis have concentrated on linear circuits (ideal operational amplifiers) or linear circuit components (R, C, L) [3, 4, 5, 6]. Typically, process or layout parameters are not taken into account as faults, and the number of faults is relatively small. Compared with previous work, we diagnose process and layout parameter faults effectively with a simplified neural network architecture in this paper.

II. Neural Networks

By far, the most popular neural network architecture is the backward error propagation (BP) neural network [4]. A comparison of five neural network architectures is provided by Hsu et al. [7]. The BP neural network provides the best results for the pattern classification task [7]. In this paper, we also adopt a BP neural network.

Neural networks are divided into two categories: supervised and unsupervised based on their learning strategies. BP neural network

is a supervised neural network. Typically, it has two or three layers of interconnecting weights. Fig. 1 shows a standard two layer neural network. BP neural network is a fully connected network topology. Every input neuron is connected to all hidden layer neurons. Every hidden neuron is connected to all output neurons similarly. Every neuron in the network has the structure shown in Fig. 2, where pi (i=0,1,2...n-1) are inputs, wi (i=0,1,2...n-1) are weight coefficients, b is the bias, f(x) is the transfer function, which must be nondecreasing and differentiable over all time. A common function is the log-sigmoid function: f(x)=1/(1+exp(-x)).

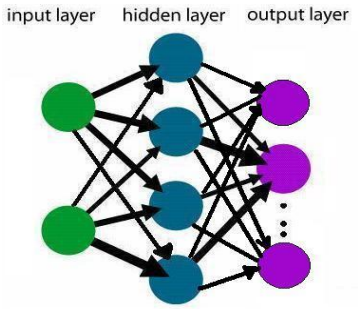

Fig. 1. A standard two layer BP neural network topology

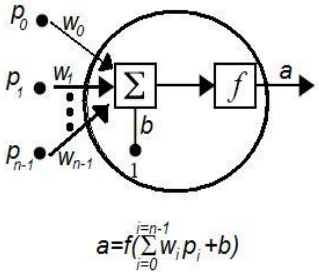

Fig. 2. Artificial Neuron

III. Design of neural network architecture

A carefully constructed network architecture can lead to excellent diagnosis results. Generally, when neural networks are used for analog circuit diagnosis purposes, measurements of analog circuits constitute the inputs of the network. A typical approach to construct the output layer is to set the number of neurons equal to the number of faults [8]. However this approach typically makes the network too complex for efficiency and result too convoluted to make a diagnosis decision.

In our method, we develop one simple neural network for each fault, and place only one neuron in the output layer of each network. The target output value is 1 or 0, increasing the range between decision boundaries. A fault resolution boundary is set to determine whether a combination of particular inputs (measurements from the circuit) belongs to the current fault class. When the network output value is bigger than fault resolution boundary, we deduce that the input scenario corresponds to the fault class. The difference between the traditional neural network architecture and ours is demonstrated in Fig.3.

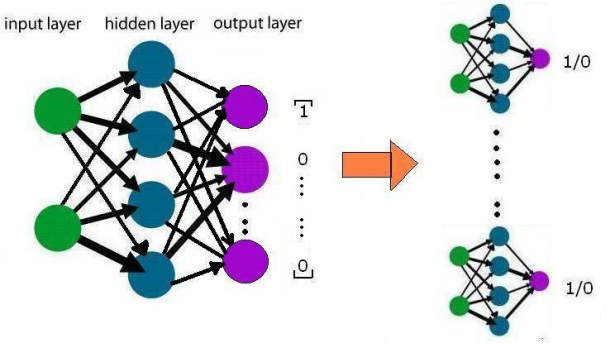

Figure3: The change of neural network architecture

We first confirm that our approach of employing multiple simple networks in place of one complex network does not lead to increased computation (training time) and space complexity. The space requirement can be analyzed analytically whereas we compare training time and diagnosis results experimentally due to the randomness involved in process variations.

A. Storage space features

We implement one small neural network for each fault, whereas in traditional neural-network based fault diagnosis, one large

network is trained to learn the behavior of all faulty circuits. To compare the space requirements, let us denote the number of inputs (measurements from the circuit) with N_t, the number of hidden layer neurons with N_h, and number of faults with N_f. A neuron needs to store one weight value for each connection, and another bias value, as shown in Fig2. Thus the storage required for the traditional architecture is:

$$S_t=(N_t+1)\times N_h+(N_h+1)\times N_f$$

The storage required for our method is:

$$S_p=((N_t+1)\times N_h+N_h+1)\times N_f$$

If $N_f>>Nt$ and $N_f >>N_h$,

$$S_t \approx N_h \times Nf = O(N_f)$$

$$S_p \approx (Nt+2)\times N_h \times N_f = O(N_f)$$

Clearly, our approach requires more space than the traditional approach. However the space requirements for both approaches have linearly complexities in terms of the number of faults. As such, we conclude that the space requirement of our approach is not prohibitive.

B. Training time

To compare the training time of our approach with the traditional neural network approach, we need to generate circuit instances. Due to the randomness in this process, the training time cannot be analyzed analytically. We present in this section an experimental comparison. We generate neural networks based on 28 faults and simulate 30 instances of each faulty circuit to take process variation into account. The faults injected in our experiments are at process level (circuit details are in section 5). For traditional neural network, we apply one network with 6-6-28 architecture, while we apply twenty-eight networks with 6-6-1 architecture for our proposed method. Training time of different architectures is shown in Table1. We also conclude that our approach requires less training time, thus using multiple neural networks does not lead to any increase in space/time complexity.

Table1. Comparison of training time of different network architecture

	Traditional architecture	Our architecture
Training time	2.2411×10^3s	0.3454×10^3s

C. Diagnosis accuracy

While we will present more detailed diagnosis results in Section 5, we would like to show that the proposed approach leads to better diagnosis results. After training the abovementioned two kinds of network architectures, we generate 280 circuit instances for testing, 10 instances for each fault. We put the same input test pattern into these two different architectures. The diagnosis result is shown as Table2.

Table2. Comparison of diagnosis accuracy of different network architecture

	Traditional architecture	Our architecture
Classification accuracy	89%	93%
Ambiguity group size	16	12

Classification accuracy is gained by calculating the ratio of right classifications to all the classifications. Ambiguity group size means the undistinguishable group size. In this case, it means after we set a fault resolution boundary, for traditional architecture, there are 16 faults, whose occurrence probability is beyond the boundary. These results indicate that while our approach does not lead to increased space/time complexity (in terms of the number of faults), the diagnosis efficiency is much better. Thus, we conclude that our approach is superior to using one complex neural network to capture the behavior of all faulty circuits.

IV. Diagnosis principle using neural network

The neural networks work as a fault dictionary, which consists of a series of feature vectors and corresponding fault classes. Feature vectors are extracted from circuit measurements. To obtain as much diagnostic resolution as possible while keeping the fault dictionary in a manageable size, we utilize sensitivity guided input selection technique to select effective measurements. In the frequency domain, the sensitivities provide information about the goodness of an input at a specific frequency location to improve the diagnostic resolution. More details of this technique can be found in [1]. After deciding the most effective frequency point, the AC gains are measured by HSPICE. We then normalize the result from the measurements to avoid skewing the results. The input feature vectors and corresponding fault classes to the neural network are paired to train the neural networks.

During the diagnosis phase, the response is measured from the circuit and all neural networks are evaluated with this response. If the response of a network is higher than a threshold (determined during the training phase), we conclude that the circuit response can be associated with the fault that is used to train that network.

V. Experiment Results

To evaluate the proposed diagnosis approach, several experiments have been conducted on a two-stage amplifier as shown in Fig. 4. At process level, $(W, L, T_{ox}, U_0, V_{t0}, \lambda)$ are considered. All the parametric faults are defined on these process level parameters.

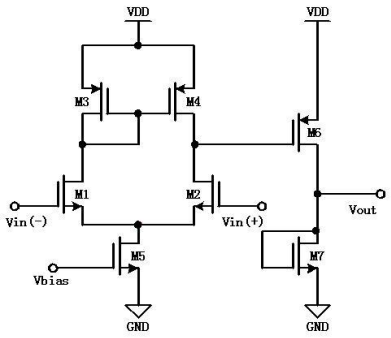

Figure 4: The two-stage amplifier used in the experiments [1]

A single fault model is used in experiments. Parametric faults are injected into the fault-free circuit by deviating the nominal values of process parameters. Each process parameter has four deviations from nominal values (+/- 20%, +/- 10%). For the non-faulty parameters in the fault circuits, small deviations (2%) are added, which is used to mimic the process variation during manufacturing.

In this case, we use one 2-layer BP neural network per fault, as shown in Fig. 1, training a 6-6-1 structural neural network by the BP algorithm. The transfer function is log-sigmoid, while mean square error (MSE) is 0.0001, and the training will not stop until the network has been trained 200 iterations or it satisfied the performance request. The 6 input layer neurons stand for the AC gain at 6 frequency points (100kHz, 5MHz, 50MHz, 200MHz, 500MHz), which is determined by sensitivity based input selection technique [1]. At the beginning, 40 Monte Carlo analyses are conducted for every faulty circuit with tolerance. 30 of them are used for training neural networks and the other 10 are for testing. To increase the diagnostic resolution, we do not only use 30 input vectors of the corresponding fault to train the network, but also add nominal response from all the other faults.

In 30-sample Monte Carlo simulation, computation time 1.9635×10^{3}s, the

classification accuracy is 95%, the ambiguity group size is 43. To shrink the ambiguity group size, increase the diagnostic resolution, 300-Monte Carlo simulation is adopted. In this case, when the classification accuracy is still 95%, the ambiguity group size declines to 26. The computation time is 2.2177×10^{3}s.

In 300-sample Monte Carlo simulation, with different boundaries of fault resolution, we get different classification accuracies and average ambiguity group sizes, shown in Fig.5 and Fig.6. After considering classification accuracy and ambiguity group size synthetically, we choose 0.95 as the fault resolution boundary.

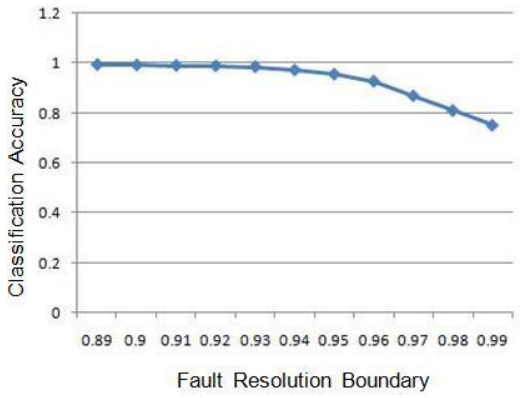

Figure 5: Classification Accuracy under different boundaries

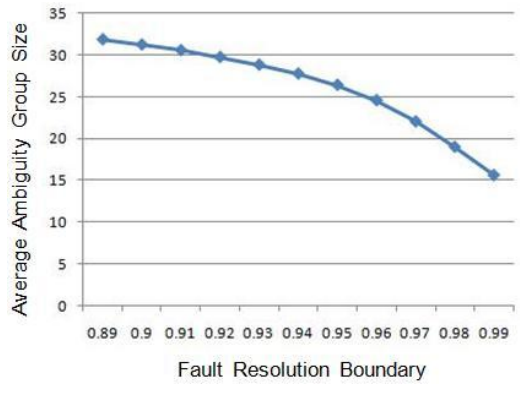

Figure 6: Average Ambiguity Group Size under different boundaries

VI. Conclusion

A fault diagnosis approach for analog circuits, based on frequency domain analysis and neural networks is provided. A new neural network architecture is developed to increase diagnostic resolution. Using 300-sample Monte Carlo simulation, our experiments on a two-stage amplifier circuit show that 95% of process level faults can be diagnosed accurately in 37 minutes, and the average ambiguity group size in 120 faults is 25.

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