Software Defined Radio Receiver Based on Six-Port Technology

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***Abstract* - Software Defined Radio (SDR) has been identified as one potential method to enhance the flexibility of wireless communication systems. In the past, the operating speed limitation of analog digital converter (ADC) and processing ability limitation of re-configurable chips for signal processing have slowed down the development of SDR for useful commercial application. With recent advances in the semi-conductor processing technology and the development of re-configurable devices such as digital signal processors (DSP) and field programmable gate arrays (FPGA), SDR has now become practical for use in system solutions including wireless LANs, audio and television broadcasting and interoperability between different radio services. In this paper, we describe the application of SDR based on Six-Port technology to provide multi-channel, multi-mode wireless digital receiver. The combination of SDR and Six-Port technology provides a great flexibility in system configuration, a significant reduction in system development cost, and also a high potential for software reuse.**

I. INTRODUCTION

Software Defined Radio (SDR) is an Information Transfer System (ITS) that combines technology from the historically separate fields of computers and radios. Emerging from military applications, SDR has been receiving much attention among researchers working on wireless communications.

The essence of an SDR is the ability, without introducing new hardware, to change operating characteristics such as operating frequency range, modulation type, bandwidth, maximum radiated or conducted output power and network protocols by changing the software programs executing in processing resources. In software defined radio, operating parameters are determined by software. This enables a single wireless device to be reprogrammed to use different modulation, coding, and access protocols.

Also, software defined radios could allow more efficient use of spectrum by facilitating spectrum sharing and by allowing equipment to be reprogrammed to more efficient modulation types. Their ability to be programmed could also enhance interoperability between different radio services. Most software radio research to date has been driven by the interoperability problems that are present in commercial and military wireless systems. Fig. 1 shows a block diagram of a Software Defined Radio Receiver. In software radio systems, the IF signal is digitized using wide-band ADC's, and all of the subsequent processing is implemented in software [1]–[5].

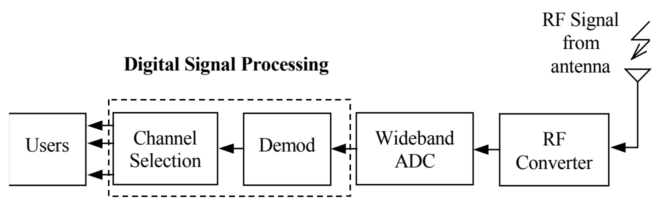


Fig.1 Block diagram of a Software Defined Radio Receiver

Today the evolution toward practical software radios is accelerating through a combination of techniques. These include smart antennas, multiband antennas, and wideband RF devices. Wideband analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) access GHz of spectrum instantaneously. Intermediate Frequency (IF), baseband, and bit stream processing is implemented in increasingly general purpose programmable processors. The resulting software-defined radio extends the evolution of programmable hardware, increasing flexibility via increased programmability. The ideal software radio represents the point of maximum flexibility programmability in this evolution.

II. RECEIVER ARCHITECTURE AND OPERATING PRINCIPLE

One key point of SDR is to have a digital processing kernel with almost infinite processing ability. Although DSP and semiconductor technology have developed rapidly in the past ten years, the operating speed level of current DSP chip can't completely support a high speed multi-channel multi-modulation SDR at IF level. Therefore certain software radio systems adopt multichips architecture and parallel algorithm, thereby increasing the design complexity and potential cost.

Instead of digitalizing signals at IF, signals can be digitalized at baseband to reduce the processing requirement for DSP chips. As a new solution of SDR design, a direct demodulator architecture, based on six-port technology, or 'multi-port demodulator', is used in our proposed RF software receiver. Signals are down converted from Radio frequency (RF) to baseband directly by a six-port module. This paper presents recent results obtained on the analysis of SDR technology in direct RF six-port receiver designed for multi-mode wireless communications.

Six-port technology was originally developed as an amplitude and phase measurement methodology for high frequency signals [6]. In 1994, Ji Li, R. G. Bosisio and Ke Wu proposed application of this technology for direct receiver [7]. In principle, the circuitry of a six-port consists of dividers and combiners interconnected in such a way that four different sums of a reference signal and the signal to be measured are produced. Different lengths transmission lines between the components, the two signals generate different phase values at output ports, resulting in constructive or destructive interference. The signal levels of the four combined signals are detected using Schottky diode detectors. By applying suitable algorithms, the magnitude and phase of the unknown microwave signal can be determined for any given modulation scheme [7],[10] from the four power values and physical calibration [8] or regenerative data calibration [9] obtained from incoming signal.

The structure of a software six-port receiver is shown in Fig.2. A block diagram of six-port circuit is also included. The circuit consists of one power divider and three hybrid couplers. Six-port circuit works as a RF down converter in the proposed receiver. Port 2 connects to RF signal and port1 connects to reference signal, the other four ports are connected with power detectors. The receiver is designed to operate at center frequency of 24 GHz and operates over a wideband of 22-26GHz for multi-mode schemes.

Consider the case at reference plan 2-2' in Fig. 2, the "incident wave" a_2 and the "reflect wave" b_2 are in frequency f_{RF}, f_{LO} and have arbitrary relative relationships φ_1, φ_2. So that:

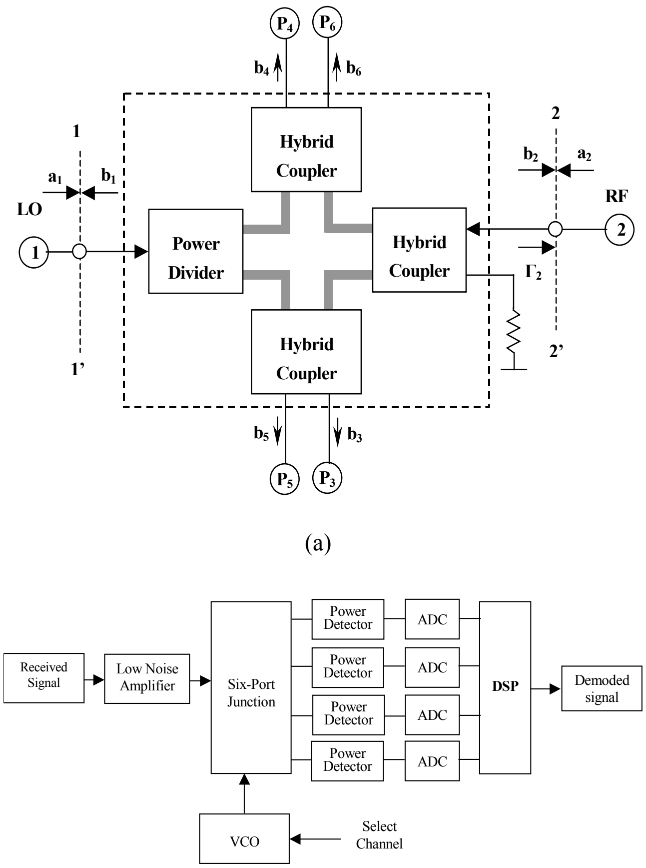
$$a_2 = |a| e^{j(2\pi f_{RF} t + \varphi_1)} \tag{1}$$

$$b_2 = |b| e^{j(2\pi f_{LO} t + \varphi_2)} \tag{2}$$

If their frequency difference is small, the S parameters of the six-port to be calibrated can be regarded as being constant at each frequency and the equivalent reflection coefficient becomes:

$$\Gamma_2 = \frac{b_2}{a_2} = \left|\frac{b}{a}\right| e^{j(2\pi\Delta f t + \Delta\varphi)} \tag{3}$$

where $\Delta f = f_{LO} - f_{RF}$ and $\Delta\varphi = \varphi_2 - \varphi_1$



(a)

(b)

Fig.2 (a) Six-port circuit (b) Architecture of software six-port receiver

The frequency difference Δf can be readily obtained from the derivative of $\theta(t)$

$$\Delta f = \frac{\theta(t_2) - \theta(t_1)}{t_2 - t_1} \tag{4}$$

where the time interval between two samples $\Delta t = t_2 - t_1$ is properly chosen for best accuracy. It is to be noted that the sign of Δf is direct indication of relative position of f_{RF} and f_{LO}. In this way, we can then know the ratio of amplitude, frequency and phase between LO signal (port 1) and RF signal (port 2) from the power output at the other four ports. Thus,

$$\Gamma_2 = \frac{\sum_{i=3}^{6}(A_i + jB_i)P_i}{\sum_{i=3}^{6}(C_i + jD_i)P_i} \tag{5}$$

where A_i, B_i, C_i, D_i are real constants that can to be known by calibration procedures.

III. RESULTS AND DISSCUSSION

The RF microstrip layout of six-port circuit is shown in Fig. 3. The circuit is fabricated in miniaturized hybrid microwave integrated circuit (MHMIC) technology on a 250µm ceramic substrate with a relative permittivity ε_r=9.9. The MHMIC chip measures 9.5x8.4 mm.

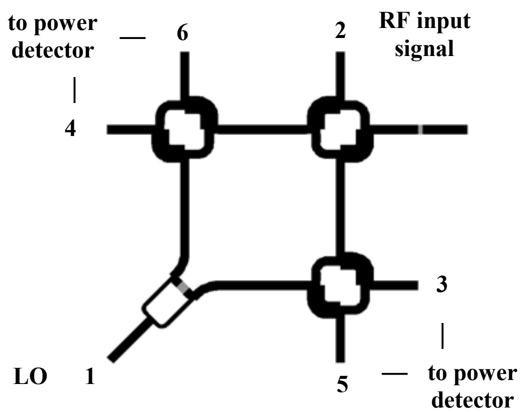


Fig. 3 Design layout of the six-port circuit

Simulated and measured S-parameters of the six-port junction are shown in Fig. 4 for the center frequency at 24 GHz. The isolation between RF and LO ports is found to be at least 22 dB. The transmission coefficients are close to the theoretical predicted value (6 dB).

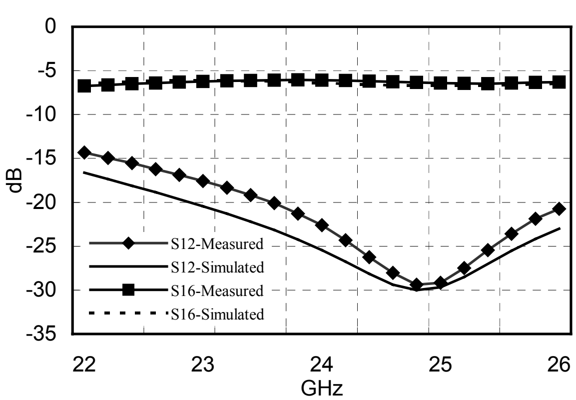
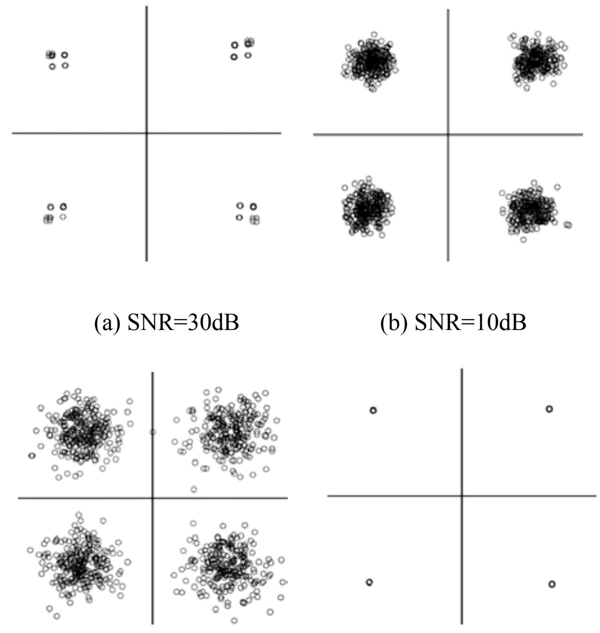


Fig. 4 Simulated and measured S-parameters of the six-port circuit

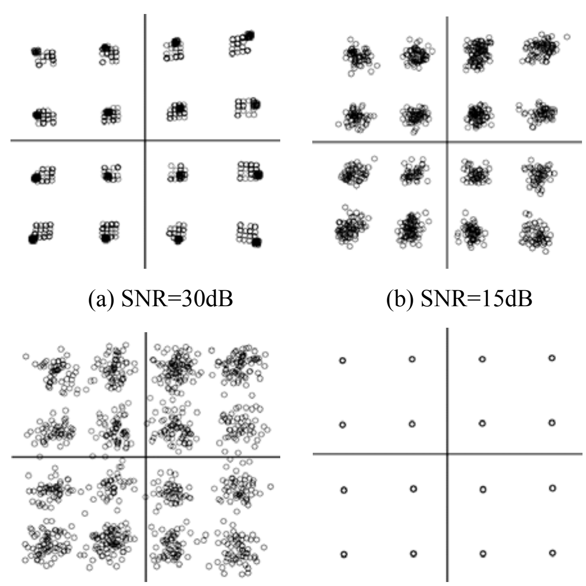
Within the operating frequency band of the receiver (22 GHz – 26 GHz), two modulation schemes (QPSK and QAM16) are selected to test the performance of the new algorithm in software receiver.



(a) SNR=30dB (b) SNR=10dB

(c) SNR=4dB (d) Demodulation result

Fig. 5 Simulated output signal constellations for QPSK with different SNR.



(a) SNR=30dB (b) SNR=15dB

(c) SNR=4dB (d) Demodulation result

Fig. 6 Simulated output signal constellations for QAM16 with different SNR.

Fig. 5 and Fig. 6 show the simulated output signal constellations for various signal-to-noise ratios (SNR). A white noise is added to the input signal and the output constellations are presented in Fig. 5 (a)–(c) for QPSK signal with SNR equal 30-, 10-, and 4-dB, Fig. 6 (a)–(c) for QAM16 signal with SNR equal 30-, 15-, and 8-dB SNR, respectively. Demodulation results are presented in Fig. 5(d) for QPSK signal and Fig. 6(d) for QAM16 signal as well.

Simulated and theoretical BER vs. E_b/N_0 for the two modulation types are presented in Fig. 7 and Fig. 8, where E_b is the average energy of a modulated bit and N_0 is the noise power spectral density. The carrier power P_{RF} is -21dbm and local oscillator power P_{LO} is -21dbm. The Bit rate of QPSK and QAM16 signals is 1Mb/s. It is seen that the simulated BER curves match the theoretical BER curves very well, the BER is less than 1E-3 for E_b/N_0 higher than 7 dB (QPSK) and 11dB (QAM16) over the frequency range within the operating band.

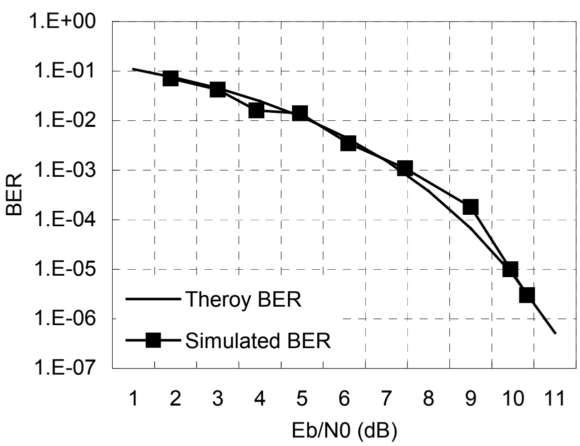


Fig. 7 Simulated and predicted BER for QPSK modulation.

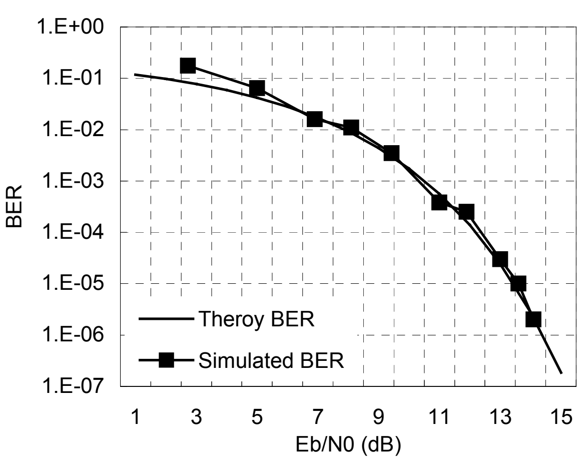


Fig. 8 Simulated and predicted BER for QAM16 modulation.

IV. CONCLUSION

The development of SDR technology based on six-port receiver scheme has been proposed and presented. The transmission characteristics are simulated using an actual hybrid integrated six-port circuit. The results of BER vs. E_b/N_0 of SDR receiver for two different modulation schemes have been described. The preliminary simulation results are very encouraging, showing a possible direct demodulator for future software defined radio terminals in various low cost communication systems.

ACKNOWLEDGEMENT

The author would like to acknowledge the National Science Engineering Research Council (NSERC) of Canada for its financial support.

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