BROADBAND RECEIVER FOR SOFTWARE DEFINED RADIO IN GIGA-HZ RANGE BASED ON 40NM SI TECHNOLOGY

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ABSTRACT-In this paper, a low voltage ultra-wideband RF receiver for Software-Defined Radio (SDR) is presented. In SDR design, the radio frequency (RF) receiver should be able to receive signals over a broad-bandwidth so that it can satisfy a variety of different communication standards. In the proposed design, working frequency ranging from 0.1GHz to 6GHz RF front-end for SDR, covering almost all of mature communication standards, is designed. Implemented in a standard 40nm CMOS technology, the proposed receiver is realized consisting of ultra-wideband low noise amplifier, active mixer, intermediate frequency amplifier and variable gain amplifier. It is able to work in the ultra-wideband while preserving low noise figure and consuming less than 5mW power under a single 1.1-V supply voltage.

Keywords- Low voltage; ultra-wideband; Software-Defined Radio

INTRODUCTION

With the rapid development of electronic information industry, RF integrated circuit (IC) becomes a research focus which attracts the attention of many experts and scholars. As one of the most important parts in RFIC, receivers play a vital role in the wireless communication market. In communication systems, electronic transmitter and receiver circuits transfer information to and from a communication medium.

The concept of SDR, which can provide the multi wireless standards with a single hardware platform, has drawn great interest of people in the academic and industry. Extensive works have been dedicated to design receivers in radio frequency range in recent years. Several prototypes have been successfully developed to demonstrate the possibility of high data-rate at a short range. Up to now, SDR have been reported in many research works [1-3] which required wideband receiver with good performance.

Different generations of wireless technologies such as DECT, Bluetooth, Wi-Fi, UWB and recently Bluetooth 2.0 all provide high speed data links and need to coexist. The concept of software-defined radio allows the utilization of one single flexible receiver hardware in multiple standards. Achieving this goal requires a wideband receiver that can work across standards instead of multiple receivers customized to work in narrow frequency bands. The programmability and configurability of SDRs are prospective advantages over traditional RF devices. Traditional RF devices either do not have or have a limited capability in programmability and configurability. With SDR, software modules define the base-band and protocol elements and provide an environment for easy application development. Without introducing new hardware, an SDR can control working parameters such as the frequency range, modulation type, bandwidth, maximum output power, on/off sensing and network protocols by programming the software. This enables a single wireless system to be reprogrammed for using different modulation, coding, and access protocols. This great flexibility of SDR provides opportunity for solving interoperability problems between many different standards, implementing new standards, and minimizing the amount of hardware necessary to perform communications across these different standards. SDR also allows more efficient use of the spectrum by facilitating spectrum sharing and allowing equipment to be reprogrammed to more efficient modulation types.

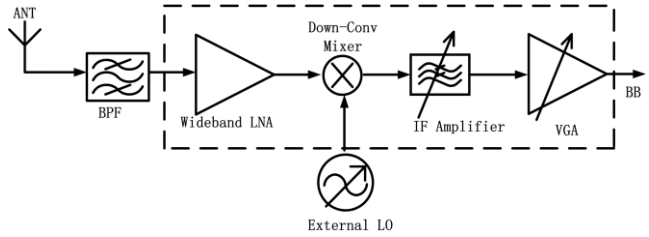
The proposed SDR receiver is realized in a 40 nm CMOS technology coving the frequency range from

0.1 GHz to 6GHz, applicable to almost all of mature communication standards. In the following sessions , the considerations of an SDR analog receiver front-end are described, followed by a detailed circuit analysis and detailed simulation results. Then the performance of the system and simulation results are presented and discussed. Conclusions are given in the final session.

DESIGN CONSIDERATIONS

For SDR receiver, it is desirable to achieve the multi-mode and multi-standard operation to satisfy requirements such as broadband, low cost, low power consumption and compatibility with digital signal processor (DSP). As has been demonstrated earlier, a direct up/down conversion architecture is the most suitable architecture to build an SDR [4]. In this paper, a frequency ranging from 0.1GHz to 6GHz is proposed for the receiver to achieve desire goals. The block diagram of the proposed SDR receiver is shown in Fig.1. The RF signals are first received from antenna (ANT), and then go though the band-pass filter. After that they are amplified by low noise amplifier (LNA) and down-converted by mixer. The down-converted signals are amplified by intermediate frequency (IF) amplifier and variable gain amplifier (VGA). Next the IF signals are sent to the analog digital converter (ADC). The digitalized signals are processed by DSP and all of the subsequent processing is implemented in software.

Fig.1. Block diagram of the proposed receiver for SDR.



Many key aspects including noise, sensitivity, linearity, power consumption should be considered when design a SDR receiver. These performances have been defined by wireless standards for communications.

Firstly, silicon based SDR wireless system is mainly used in medium distance. The typical signal power can be as low as -70dBm. Secondly, as the receiver should be universal, the working band should be broad, for example, from 0.1GHz to 6GHz. It should be able to obtain data-rate from kbps to tens of Mbps. Simple modulation schemes, e.g. ASK, OOK and complex modulation schemes such as OFDM can be applied in the receiver system. On the other hand, the requirement of linearity in the band range should be well controlled as well.

As shown in Fig.1, taking into account the image rejection, the system should be designed with I and Q paths. Fig.1 demonstrates one of them. A down-conversion receiver with the output of IF signal of 1Mbps is implemented. The minimum input power (sensitivity) is less than -90dBm. The signal gain of the whole system is higher than 50 dB, and the power consumption is less than 5mW. The receiver front-end as shown in the frame includes LNA, mixer, IF amplifier and variable gain amplifier. External local oscillator (LO) from 0.1GHz to 6GHz will be used in the measurement. .

For this design, a wideband from 0.1GHz to 6GHz LNA becomes a great challenge due to the influence of the parasitic capacitors. Low noise figure and high RF signal gain is essential to the subsequent circuits because the level of noise mainly depends on the first stage of receiver. The down-conversion mixer receives two-path signals: one comes from the output of LNA and the other is from external LO. IF amplifier with low pass filter (LPF) and VGA play a role in rejecting high harmonics and enhancing the demodulated signal. VGA also can decrease the amplitude of signal when the input signal is very strong.

CIRCUITS ANALYSIS AND SIMULATION

In this section, each circuit block of the proposed

receiver will be discussed and the simulation results will be demonstrated.

Wideband LNA

As the first stage of receiver, LNA is generally used to deal with the RF signals at required frequency. For SDR receiver, LNA is very important because it is necessary to receive all the signals in a wideband from 0.1GHz to 6GHz. If multiple narrowband LNAs were used to achieve the same functions, it would cost a lot of chip area because of every narrowband LNA requires a few inductors, which consume much chip area. In order to decrease cost, numerous wideband LNA topologies [5-7] have been reported in literatures. Two techniques including active feedback [8] and thermal noise canceling [9] were generally used. In the proposed design, noise canceling wideband LNA with current reuse technique is implemented.

The schematic of wideband LNA is shown in Fig. 2 with 50 ohm input impendence. Thermal noise canceling technique [9] is used in the proposed design. . Simulation results of the wideband LNA are shown in Figs. 3-6. As shown in Fig. 3, the noise figure is less than 2.2dB in the overall wideband. Fig. 4 presents that S11 is smaller than -12 dB and Gain is about 13 dB. Fig. 5 shows that the gain of the LNA is larger than 11.5dB in the working band. The IIP3 is larger than -5dBm over the whole 0.1GHz-6 GHz, as illustrated in Fig. 6. The power of this wideband LNA is 3mW.

Fig.2. The schematic of the wideband LNA.

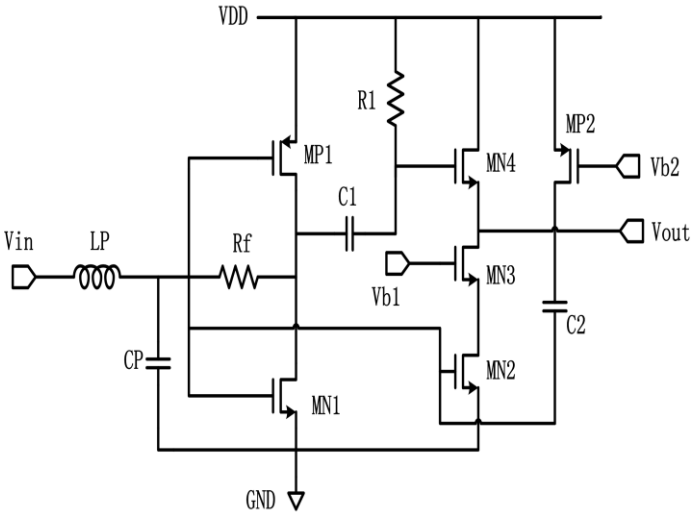


Fig.3. Noise figure of the proposed LNA.

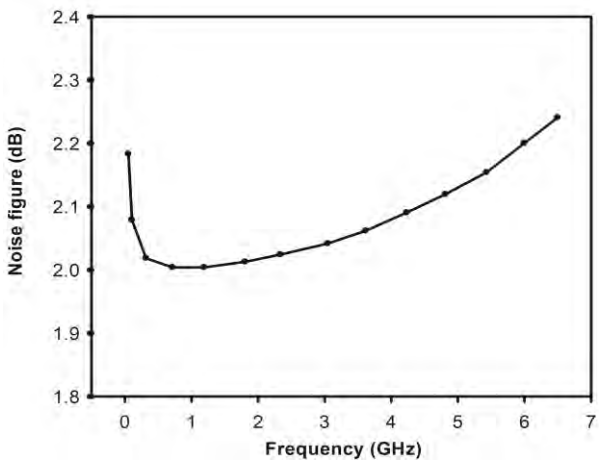


Fig.4. S11 for the proposed LNA as functions of frequency.

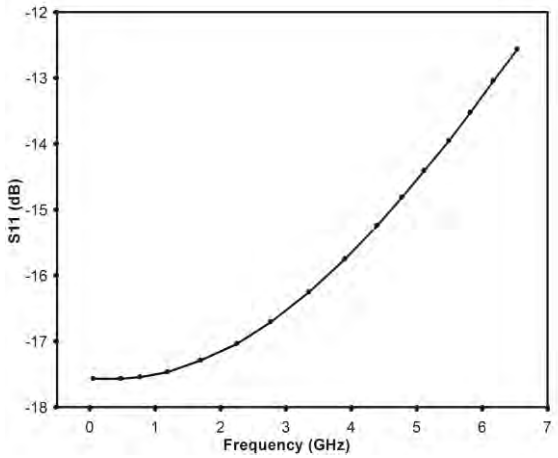


Fig.5. Gain for the proposed LNA as a function of frequency.

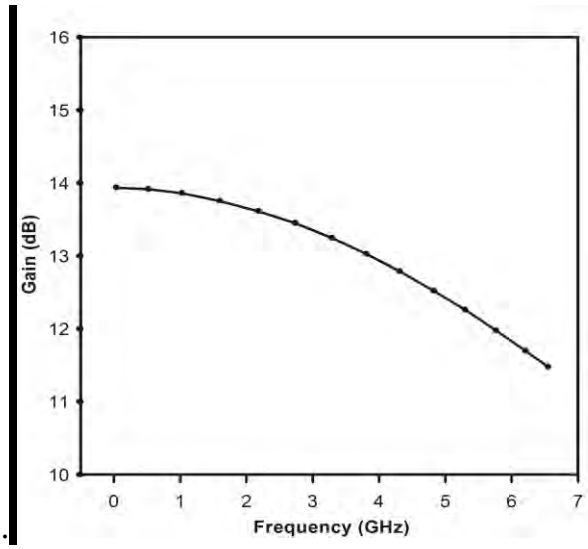
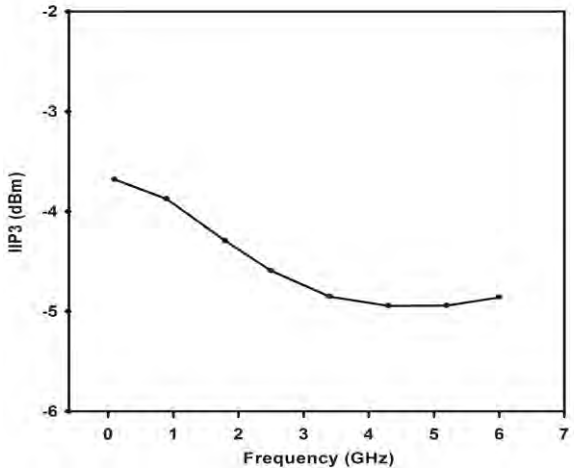


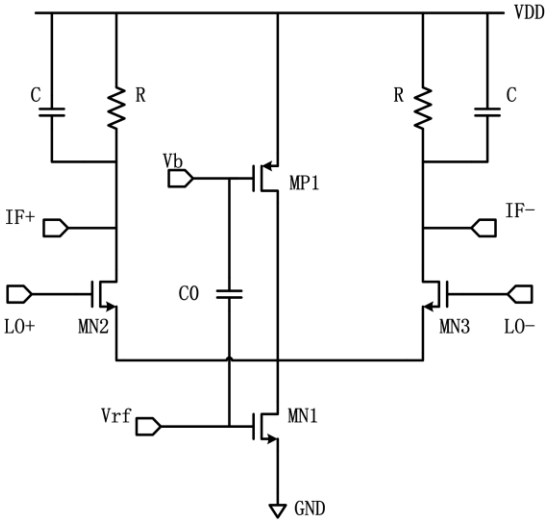
Fig.6. Two-tone IIP3 of LNA.



Active mixer

Compared with active mixers, passive mixers do not have static power consumption, but its conversion gain is less than 1. In this design, active mixer is used to improve the gain of receiver. The proposed active mixer is shown in Fig.7. The proposed mixer can provide conversion gain of 8dB, and the isolation from LO to IF is -58dB. The mixer has NF of 8.5dB and power consumption of 1.27mW.

Fig.7. The schematic of active mixer.



IF amplifier

After the demodulation, the output signal from mixer locates in IF range at 1MHz. In order to filter out high harmonics and enhance the demodulated data, IF amplifier is used as shown in Fig.8. The IF amplifier with appropriate value of resistors R1 and R2 has an AC gain of 20dB and bandwidth of 2MHz.

VGA

Variable gain amplifier is widely used in RF receivers to improve the dynamic range of the overall system. There are two approaches used to realize VGAs depending on the control signal. VGA controlled by analog signals [10] takes the advantage of variable transconductance and the gain can be controlled continuously. A digitally controlled VGA [11] would simplify the circuit and the gain varies as a discrete function of the control signal. The simplified schematic of digitally controlled VGA is shown in Fig.9. The gain is equaled to N or 1/N which are the ratio of feedback resistor to input resistor. According to requirement, the number of resistors would be carefully selected to control the gain range. A VGA gain ranges from -12 to 12 dB with 6 dB per step is implemented in the present work.

Fig.8. The schematic of IF amplifier.

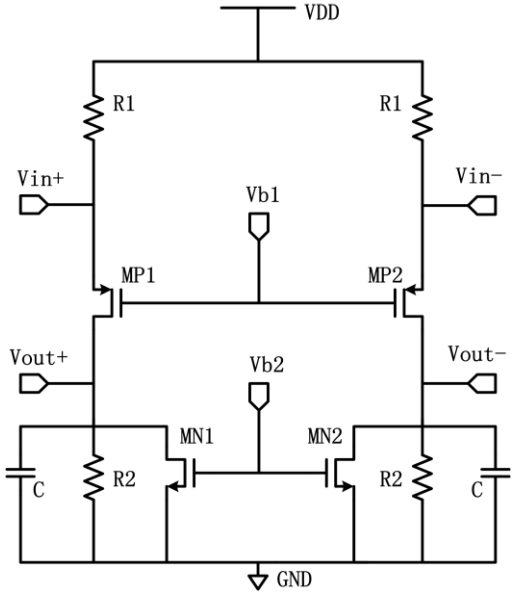
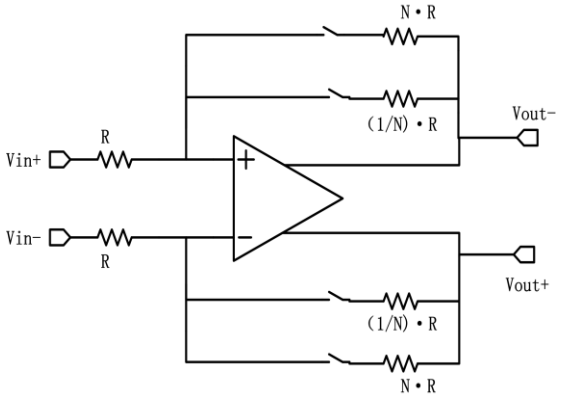


Fig.9. The schematic of variable gain amplifier.



SDR RECEIVER SYSTEM

In this section, the system simulation results are presented and analysis is made. The noise figure of the receiver is shown in Fig.10. It ranges from 3.0dB to 5.2 dB over the bandwidth range. The input signal has a data rate of 1 Mbps with 0.1GHz to 6 GHz carrier. The gain of the system can attain more than

50 dB. Fig.11 shows the layout of the wideband (0.1GHz to 6GHz) receiver. The silicon area of the receiver is bondpad-limited. The effective area is 0.045mm^2. The signal input by utilizing a ground-signal-ground (GSG) structure and the measurement of differential output by a ground-signal-signal-ground (GSSG) structure. A series of 7-pin eye pass pads are used for DC biasing. The proposed system has a wide operating frequency range from 0.1GHz to 6GHz with an input signal ranging from -90dBm to -30dBm. The total power consumption can be as low as 5mW.

Fig.10. The noise figure of proposed SDR receiver.

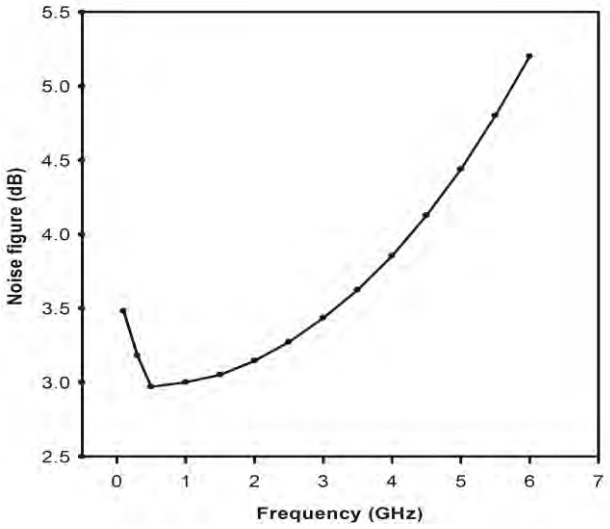
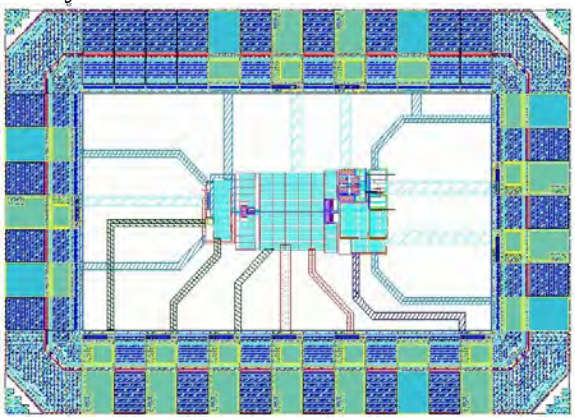


Fig.11.Layout of the receiver



CONCLUSION

This paper proposes a SDR receiver front-end in a standard 40 nm CMOS technology. The receiver is based on a low-IF architecture with a data rate of 1 Mbps and it is able to cover 0.1G-6GHz frequency range. The DC power consumption of the whole system is less than 5mW from a 1.1V supply. Additionally, energy scalability can be further achieved by balancing power and performance.

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