Relationship Between ADC Performance and Requirements of Digital-IF Receiver for WCDMA Base-Station

Hae-Moon Seo, Chang-Gene Woo, and Pyung Choi

***Abstract*—The recent rapid development of digital wireless systems has led to the need for multistandard, multichannel radio-frequency (RF) transceivers. This paper presents the relationship between the performance of a bandpass-sampling analog-to-digital converter (ADC) and the requirements of a digital intermediate-frequency receiver for a wide-band code-division multiple-access (WCDMA) base station. As such, the ADC signal-to-noise ratio (SNR), the derivation of receiver sensitivity using the SNR/spurious free dynamic range (SFDR) of the ADC, the effect of the ADC clock jitter and receiver linearity, plus the relationship between the receiver IF and the ADC sampling frequency are all analyzed. As a result, when a WCDMA base-station receiver has a data rate of 12.2 kbps, bit error rate (BER) of 0.001, and channel index k of five (sampling frequency of 122.88 MHz and IF of 92.16 MHz), the performance of a bandpass-sampling ADC was analytically determined to require a resolution of 14 bits or more, SNR of 66.6 dB or more, SFDR of 86.5 dBc or more, and total jitter of 0.2 ps or less, including internal ADC jitters and clock jitters.**

***Index Terms*—Analog-to-digital converter (ADC), bandpass sampling, clock jitter, multistandard, receiver, signal-to-noise ratio (SNR), spurious free dynamic range (SFDR).**

I. Introduction

The market for digital radio-frequency (RF) communication is constantly expanding with the development of new services and applications. Application systems, such as cordless, cellular IMT2000 phones and wireless local-area networks, utilize a spectrum ranging from 800 MHz to 2.5 GHz. This wide variety of applications has led to an explosion of communication standards with different modulation schemes, channel bandwidths, dynamic ranges, and so forth. In addition, users are demanding low cost, low power, and small size systems to satisfy these communication standards. As a result, recent efforts to adopt a multistandard RF communication standard have focused on [1] and [2]. This technical process, which includes high-performance digital signal-processing devices such as digital signal processors (DSP) and field-programmable gate arrays (FPGAs), allows for the efficient implementation of software-defined radio (SDR) modems [3]. SDR is a radio interface technology that generally consists of a software-reconfigurable hardware platform and software modules that can make flexible changes in the hardware platform for a specific radio system application. SDR can support a variety of radio systems with multiple specifications, based on altering the software modules within a single set in the transmitter/receiver hardware platform [4].

To realize a multistandard receiver for SDR, the channel selection technique must be accomplished within a digital domain that facilitates programmable filtering. However, channel selection in a digital domain requires careful attention because of the close relationship between the analog-to-digital converter and the receiver specifications. Generally, a sigma-delta modulator (SDM) using an oversampling technique has been used in narrow-band receiver applications, such as GSM, whereas a bandpass analog-to-digital converter (ADC) using an undersampling technique has been applied in wide-band receiver applications, such as wide-band code-division multiple-access (WCDMA).

This paper presents an analysis of the relationship between the performance of a bandpass-sampling ADC and the requirements of a digital intermediate frequency (IF) receiver for a wide-band CDMA, universal mobile telecommunication system (UMTS), base station.

The rest of this paper is organized as follows. Section II describes various channel selection techniques related to a multistandard receiver. The basic architecture of a digital IF receiver is presented in Section III. Section IV outlines the relationship between the IF and the ADC sampling frequency. Section V discusses the derivation of the signal-to-noise ratio (SNR) of the bandpass-sampling ADC, while Section VI presents the calculation of the receiver sensitivity based on the SNR and spurious free dynamic range (SFDR) of the ADC. The linearity specification required in the RF/IF section is presented in Section VII, then some final conclusions are offered in Section VIII.

II. Channel-Selection Schemes

The programmability of channel selection filtering is one of the most important issues in the implementation of a multistandard receiver. Furthermore, according to the implementation method, careful attention is also needed regarding the influence on the required specifications of the RF/IF/baseband stages. Fig. 1 shows examples of receiver requirements according to various channel-selection schemes, including analog, digital, and mixed-signal methods. These schemes must be able to satisfy the system, RF/IF, and digital requirements. Examples of system requirements include programmability, power dissipation, size, and cost. The RF/IF requirements include a dynamic range for received signals, the number of channels, worst case signal power, relative strength of the adjacent channel power, required SNR, and ADC/automatic gain control (AGC) requirement. The digital requirements include a dynamic range (DR) for the ADC, bandwidth (BW), AGC requirements, modulation scheme, and processing speed of the digital device.

Fig. 2 shows various channel-selection schemes for a receiver. Fig. 2(a) illustrates the architecture for analog channel selection. This scheme satisfies the RF/IF requirements, such as adjacent channel interferers and receiver dynamic-range problems, using a surface aquatic wave filter and AGC in the analog domain. Also, for bit error rate (BER) requirements, the resolution bit for the ADC is determined by a modulation scheme and the dynamic range of the AGC is less than 10 bits. However, this scheme, which includes fixed channel-selection filtering, has a disadvantage in that it cannot process multistandards and multichannels.

Fig. 2(b) presents the architecture of digital channel selection, which is processed using an SDM in a digital domain. This architecture can produce a multistandard receiver due to the programmability for channel selection. In addition, this architecture can provide low-pass filtering that rejects any noise pushed into a high-frequency region, adjacent-channel interferers, plus decimation of oversampling data to the converter using Nyquist-rate data. In this case, the ADC-resolution bits are determined by the SNR based on the blocking signal and noise requirements. Generally, it requires a resolution of 14–16 bits for a narrow-band application. Oversampling SDMs have already been used for narrow-band applications; however, they need a higher sampling frequency for wide-band applications. As such, undersampling SDMs can be used for wide-band systems, as WCDMA.

Fig. 2(c) presents the architecture for mixed-signal channel selection. Here, channel selection filtering is attained in the digital domain, thereby placing the burden of channel selection on the analog

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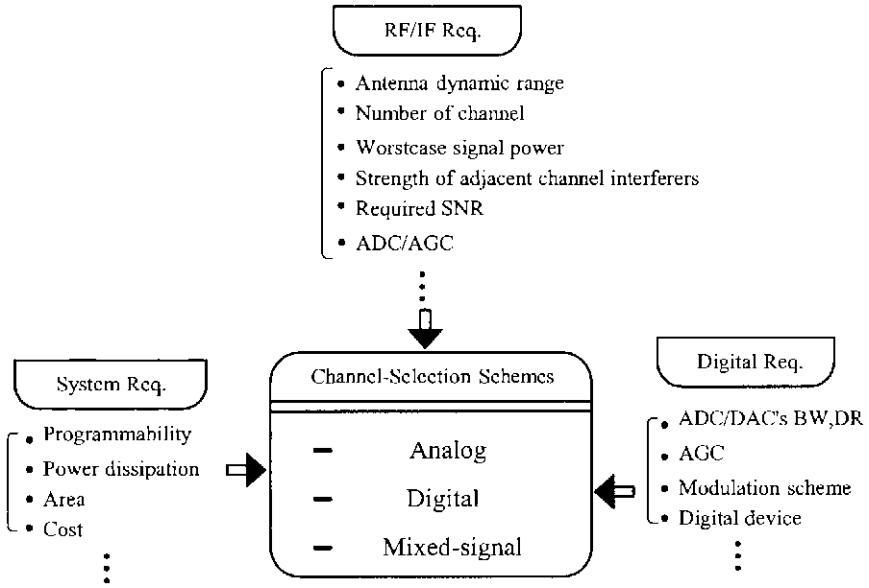


Fig. 1. Requirements for channel selection schemes.

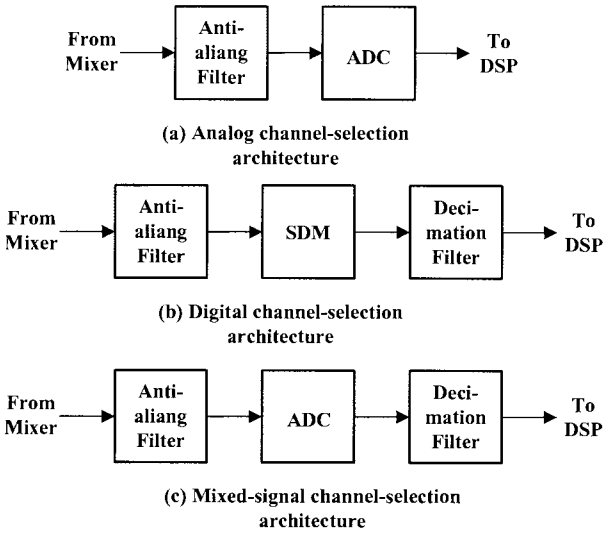


Fig. 2. Various channel selection methods.

and digital blocks simultaneously, in contrast with the methods in Fig. 2(a)and(b) The specification of the antialiasing filter is looser than that in (a) yet tighter than that in (b). The architecture uses a bandpass sampling ADC that requires 12–14 resolution bits, which is in between (a) and (b). The ADC requirements for this architecture are closely related with the ADC sampling frequency. Since channel-selection filtering is achieved in a digital domain, as in (b), a multistandard receiver can be realized using this architecture, as it provides programmability. This paper discusses a digital IF receiver using mixed-signal channel selection as in (c).

III. Architecture of Digital-IF Receiver

Conventional superheterodyne receivers use an analog channel selection scheme; however, this has weaknesses when implementing an SDR multistandard multiband receiver. Therefore, the alternative architectures of digital-IF, direct-conversion, and wideband double-IF receivers have been extensively researched for the SDR concept.

The process of channel selection in a digital-IF receiver is achieved in a digital domain, thereby avoiding the burden of RF/IF filter components. Also, channel selection in a digital domain enables the realization of the multistandard and multiband qualities of SDR. The basic architecture of a digital-IF receiver is shown in Fig. 3. In this architecture, IF signals are digitized by a bandpass-sampling ADC with a high-speed, high-resolution, and low-noise performance. The bandpass-sampling theory can be utilized in this receiver because the desired signal is a bandpass signal. This ADC can avoid aliasing caused by unwanted signals by selecting a reasonable IF, while the sampling frequency plays a role in the frequency down-conversion based on the use of frequency replicas of the desired signal bandwidth. In addition, the ADC has an influence on deciding the clock frequency and decimation factor of the digital filter. As such, the selection of a reasonable IF and sampling frequency is important. The dynamic range (DR) and spurious characteristics determined by the ADC affect not only the receiver sensitivity but also the specification of important components in the RF/IF block. In Fig. 3, the digital down-converter (DDC) consists of a digital quadrature mixer, digital oscillator, and decimation finite impulse recursive (FIR) filters. This block performs down-conversion to the baseband, plus has a duty to lower the speed of a fast wanted signal bandwidth by decimation filtering. The programmable channel selection block (PCSB) performs channel selection of the desired signal bandwidth using digital FIR filters. In a multiband and multistandard application, the PCSB performs channel selection after shifting to the baseband using a quadrature digital mixer and oscillator.

IV. Relationship Between Intermediate Frequency and ADC Sampling Frequency

According to the sampling of the analog signal, the digital spectrum is repeatedly expressed within the period of the sampling frequency based on sampling theory. Fig. 4 shows the relation between the sampling frequency and the IF for an undersampling ADC application. The proper IF location for the given sampling frequency is shown in Fig. 4(a), whereas Fig. 4(b) shows the results of an inappropriate IF location, i.e., distortion and loss of the desired signal due to the spectrum-overlap phenomenon. To sample the desired signal without

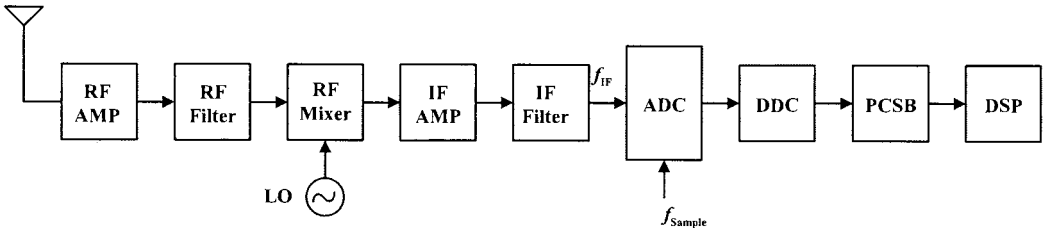


Fig. 3. Basic architecture of Digital-IF Transceiver.

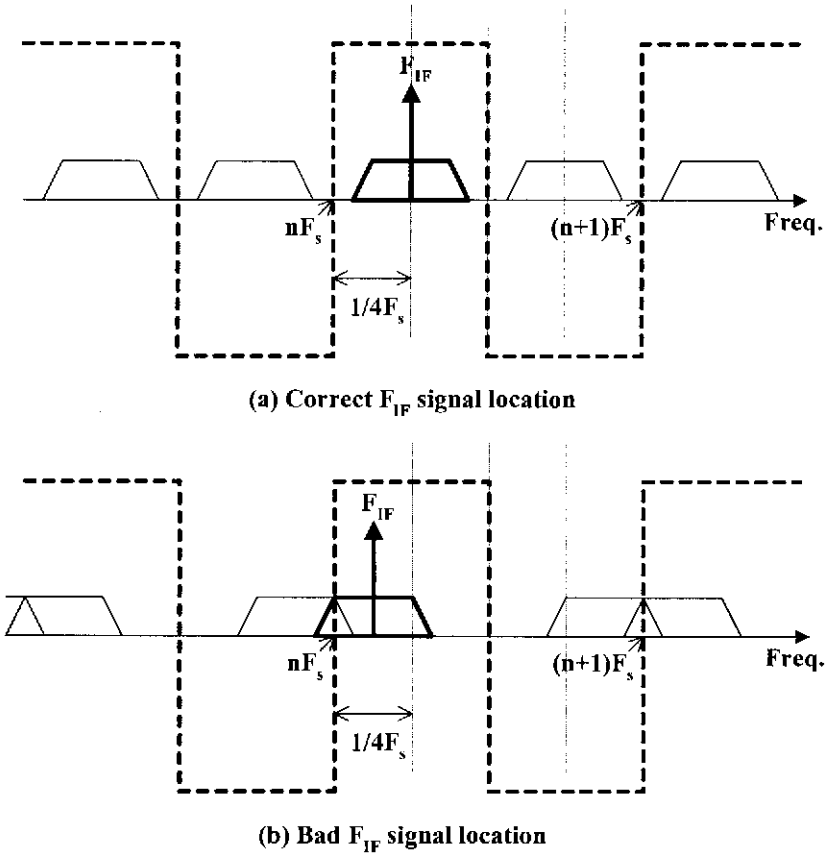


Fig. 4. F_{IF} location.

a spectrum overlap, the relation between the sampling frequency and the IF is presented by (1)

$$F_{\mathrm{IF}}[Hz] = nF_S \pm \frac{F_S}{4} \quad (n = 1, 2, 3, \ldots). \tag{1}$$

Here, the spectrum overlap is minimized when the IF (F_{IF}) is located based on a quarter of the sampling frequency (F_S). The F_S is expressed in (2).

$$F_S[Hz] = 2^k \times \mathrm{BW} \quad (k == 1, 2, 3, \ldots). \tag{2}$$

Here, k is defined as the channel index, which has an effect on the decimation factor of the digital filters used in the DDC and PCSB. To realize a multistandard receiver, F_S must be shared among the many standard specifications for each bandwidth. For example, in a WCDMA (UMTS) application with a 3.84-MHz bandwidth, an F_S of 122.88 MHz can be used along with an F_{IF} of 92.16 or 153.6 MHz (when $k = 5$, $n = 1$). The selection of k must be carefully considered when the number of multichannels is determined. Since F_S offers a processing gain by oversampling an ADC, its selection plays a role in deciding the receiver sensitivity.

V. SNR of Bandpass-Sampling ADC

A. Bandpass-Sampling ADC

A bandpass-sampling ADC in digital-IF receiver architecture performs oversampling for the bandwidth of a wanted signal, yet undersampling for IF. The oversampling of an ADC in a digital domain offers an effective processing gain ($PG_{\mathrm{oversampling}}$) for the ADC-SNR, as shown in (3). In contrast, the undersampling of an ADC essentially lowers the SNR[5]

$$PG_{\mathrm{oversampling}}\ [\mathrm{dB}] = 10 \log \left(\frac{0.5 f_S}{\mathrm{BW_{CH}}} \right). \tag{3}$$

Assuming a uniform total noise in the digitization process, faster signal samples will lower the noise floor because the noise is spread out over wider frequencies. The noise floor of an ADC can be expressed by (4)

$$\text{Noise floor} = \mathrm{FSR} - \left[6.02\mathrm{ENOB} + 1.76 + 10 \log \left(\frac{f_S}{2} \right) \right]. \tag{4}$$

Here, the effective number of bits (ENOB) is defined as the required number of bits whereby the noise power of an ideal ADC is equal to the noise power of a real ADC. The full-scale range of an ADC is

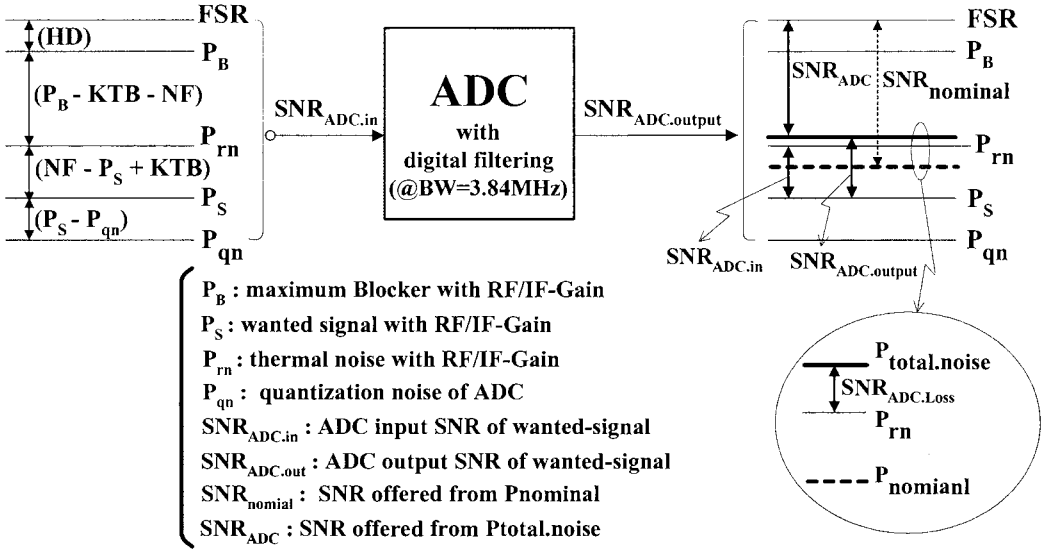


Fig. 5. Signal levels of ADC input/output.

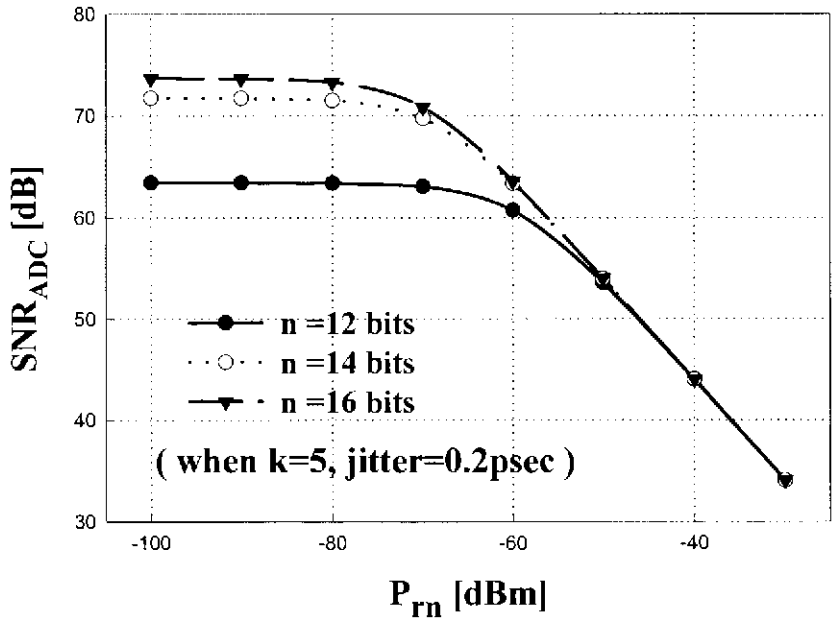


Fig. 6. $\mathrm{SNR_{ADC}}$ versus ADC input-referred receiver noise power (P_{rn}).

represented by the free spectral range (FSR). This noise consists of quantization noise and residual noise. Generally, the bandpass-sampling ADC-SNR can be easily calculated based on the resolution bits as shown in (5) [6]

$$\text{SNR [dB]} = 6.02N + 1.76 + 10\log\left(\frac{f_S}{2f_{\max}}\right) + PG_{\text{oversampling}}. \quad (5)$$

Also, this equation shows that the SNR increases when the input signal is oversampled, in contrast to the Nyquist frequency $(f_{\text{Nyquist}} = 2f_{\max})$, yet decreases when it is undersampled.

A bandpass-sampling ADC is able to directly digitize an RF/IF signal in a RF-receiver system because the desired signal is a bandpass signal. As such, a bandpass-sampling ADC performs the same function as a second mixer in a conventional superheterodyne receiver because it can down-convert the frequency by inducing a frequency replica of the desired signal bandwidth. Also, it can produce a better performance with a lower power consumption and lower cost than a conventional Nyquist-sampling ADC by using low-sampling frequency, even though it requires a bandpass filter with a steep rolloff factor offering bandlimited filtering. The analog input bandwidth of this ADC has to guarantee the $f_{\max}$ of the wanted signal. Generally, the ADC-SNR decreases as the analog input bandwidth increases.

B. ADC-SNR

Quantization methods include uniform, logarithmic (A-law, u-law), adaptive, and differential quantization. Gene-rally ADCs using uniform quantization are most widely utilized; however, this method induces a certain quantization error when representing an analog signal with a finite number of discrete amplitude levels. Assuming that this error signal is uniformly distributed among the quantization levels, the quantization noise power (P_{qn}) can be represented by (6) [7]

$$P_{qn}\ [\text{dBm}] = \frac{q^2}{12R}, \quad q = 1\ \text{LSB} = \frac{\text{FSR[V]}}{2^{\text{n}}}. \quad (6)$$

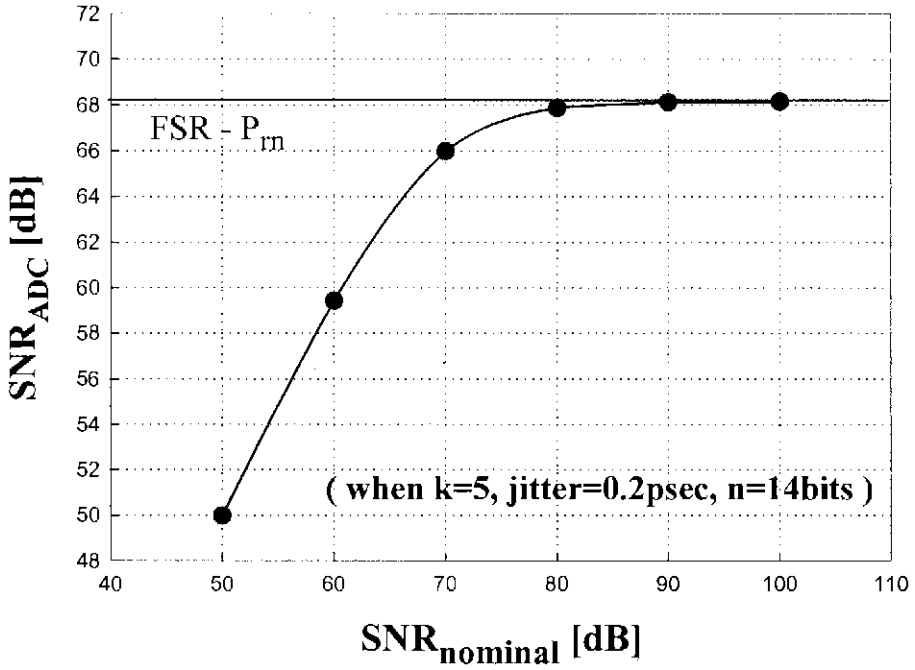


Fig. 7. $\mathrm{SNR_{ADC}}$ versus SNR.

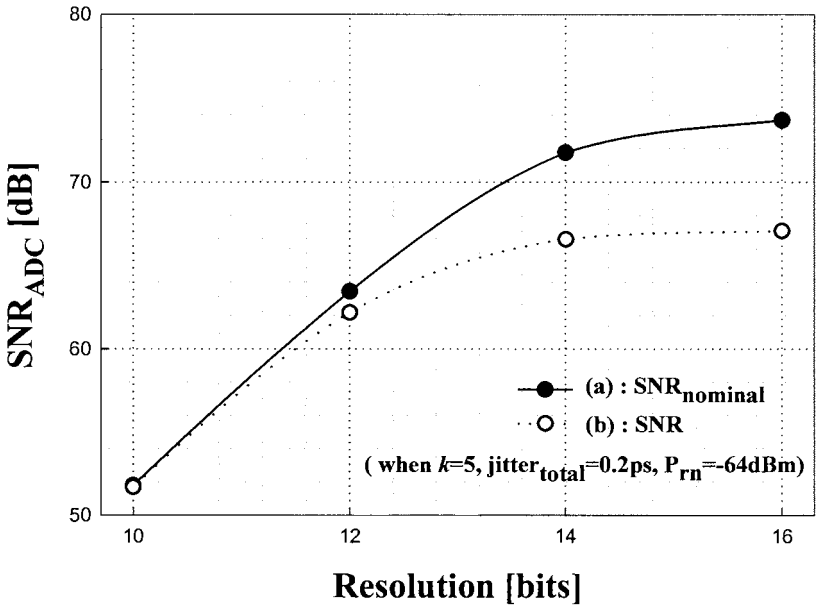


Fig. 8. Relationship between $\mathrm{SNR_{ADC}}$ and resolution bits.

Here, q is the quantization step size, R is the input resistance, and FSR is the full-scale range of the analog input-voltage range of the ADC. In ideal ADCs, the quantization noise power in (6) can be expressed when it is uncorrelated with a sampling clock. Yet, in a real situation, the SNR is decreased with an increase in the ADC total noise because the sampling-clock jitters correlate with the internal jitter of the ADC.

Fig. 5 shows the signal levels of the ADC input/output. The total noise power of the ADC output $(P_{\mathrm{total.noise}})$ contains both the nominal noise power (P_{nominal}) generated by the ADC itself and the ADC input-referred receiver noise power (P_{rn}). As such, the SNR of the ADC is determined by the $P_{\mathrm{total.noise}}$. Here, the SNR degradation of the desired signal during the ADC process should also be noted.

For a noise-limited receiver, the ADC input-referred receiver noise power (P_{rn}) is shown (7) [7]

$$\begin{aligned} P_{rn}\ [\mathrm{dbm}] &= KTB + NF + \mathrm{Gain} \\ (\mathrm{Gain} &= \mathrm{FSR} - P_B + NF, KTB \\ &= -174\ \mathrm{dBm} + 10\log \mathrm{BW}). \end{aligned} \tag{7}$$

In this case, BW is the bandwidth of the desired signal, NF is the system noise figure of the receiver, and Gain is the path gain of the RF/IF. Generally, when the harmonics and spurs of the input signal increase at the output of the ADC, various dither techniques with special circuits have been used to remove such unwanted distortion components. However, these dither methods add additive white Gaussian noise (AWGN) to the input terminal of the ADC. Similar to this concept, the harmonics and spurs induced by the quantization noise level and differential non-

linearity (DNL) error can also be somewhat minimized as the receiver noise power of the ADC input terminal, which is much stronger than the quantization noise power of the ADC. Yet, it should be noted that P_{rn} has a significant influence on the degradation of the ADC-SNR.

In the design of a GSM receiver, the SNR of the desired signal is positive ($\cong +8$ dB) because the desired-signal power from the antenna is stronger than the thermal noise power. As such, the SNR loss generated by the analog-to-digital conversion process is small enough to ignore if the P_{qn} of the ADC is as weak as 20 dB or more than P_S. However, in the design of a WCDMA receiver, the SNR of the desired signal is negative ($\cong -18$ dB) because the CDMA desired-signal power before the digital demodulation process is much weaker than the thermal noise power; see Fig. 5. As such, if only the Pqn of the ADC in a WCDMA receiver application is weaker than PS, as (8), the SNR loss of the ADC can be theoretically ignored

$$P_S > P_{qn}. \tag{8}$$

From (8), the resolution or quantization noise level of the ADC can be slightly relaxed.

In addition to P_{qn}, $P_{\text{nominal.noise}}$ considered together with other noise components, such as random noise, nonlinear distortion, and jitter effect, must be much bigger than P_{qn}. In (9), $P_{\text{nominal.noise}}$ consists of summing P_{qn}, any jitter effect, and $P_{\text{other\_noise}}$, including random noise, nonlinearity distortion, and so on. As such, $P_{\text{total.noise}}$ represents the summation of $P_{\text{nominal.noise}}$ and P_{rn}

$$\begin{aligned} P_{\text{nominal.noise}}\ [\text{dBm}] &= \sum (P_{qn} + P_{\text{jitter}} + P_{\text{other.noise}}) \\ P_{\text{total.noise}}\ [\text{dBm}] &= \sum (P_{\text{nominal}} + P_{rn}). \end{aligned} \tag{9}$$

In this paper, $P_{\text{other.noise}}$ is only assumed as a DNL effect.

The nominal SNR ($\text{SNR}_{\text{nominal}}$), considering $P_{\text{nominal.noise}}$ and the effect of undersampling, is represented approximately (10)

$$\begin{aligned} \text{SNR}_{\text{nominal}} &= \sum \left[20 \log \left(\frac{\text{signal}}{\text{noise}} \right) + \text{undersampling.effect} \right] \\ &= 2 \log \left(\text{FSR} \left[(2\pi F_{\text{IF}} \times t_{\text{total.jitter}})^2 + \left(\frac{1+\varepsilon}{2^n} \right)^2 \right]^{-0.5} \right) \\ &\quad + 10 \log \left(\frac{F_{\text{sampling}}}{2(F_{\text{IF}} + 0.5\ \text{BW})} \right). \end{aligned} \tag{10}$$

Here, F_{IF} is the analog IF of the ADC input terminal and $t_{\text{total\_jitter}}$ is the summation of the root mean square (rms) value with the internal jitter of ADC and the sampling clock jitter. The average DNL is defined as ε and $\mathbf{n}$ is the resolution-bits of the ADC. The ADC-SNR (SNR_{ADC}), considering $\text{SNR}_{\text{nominal}}$ and the effect of P_{rn}, is represented approximately by

$$\begin{aligned} \text{SNR [dB]} &= \sum (\text{SNR}_{\text{nominal}} + P_{rn}.effect) \\ &= 20 \log \left(\text{FSR} \left[(2\pi F_{\text{IF}} \times t_{\text{total.jitter}})^2 + \left(\frac{1+\varepsilon}{2^n} \right)^2 + (V_{rn})^2 \right]^{-0.5} \right) \\ &\quad + 10 \log \left(\frac{F_{\text{sampling}}}{2(F_{\text{IF}} + 0.5\ \text{BW})} \right) \end{aligned} \tag{11}$$

where V_{rn} represents the ADC input-referred receiver noise voltage of the rms value.

In the real design of a digital-IF receiver with a high nominal ADC-SNR without an automatic gain-control amplifier (AGC) loop, V_{qn} can be neglected because it has a much smaller value than V_{rn}. Based on (11), the consideration of whether the ADC-SNR will be dominated by the P_{rn} in a digital-IF receiver application can be determined using an ADC with a wide dynamic range. Accordingly, although an ADC with a high number of resolution bits offers a high nominal SNR, a real ADC-SNR in such receiver applications cannot be quarantined as such.

Fig. 6 shows the SNR_{ADC} according to the P_{rn} and ADC resolution. The value of P_{rn} can be altered by a few decibels based on the system noise figure of the receiver because G_{RF} is decided by a maximum blocker, as in (7). As the dither effect increases with the growth of the NF, the SFDR of the ADC is improved, yet the SNR_{ADC} is decreased. Fig. 7 shows the relationship between the $\text{SNR}_{\text{nominal}}$ and the SNR_{ADC} of the ADC, assuming a channel index k of 5, 0.2-ps jitter effect, and resolution of 14 bits. Since P_{nominal} is lowered with an increase in the resolution bits, $P_{\text{total.noise}}$ approaches P_{rn}, then SNR_{ADC} is saturated with FSR$-P_{rn}$ [dB], as shown in Fig. 7. Fig. 8 shows the variation of SNR_{ADC} according to the resolution bits of the ADC, assuming a 0.2-ps jitter effect, 0.5 least significant bit DNL, 92.16 MHz F_{IF}, and 122.88 MHz F_S. In Fig. 8, curve (a), the $\text{SNR}_{\text{nominal}}$ is shown when only $P_{\text{nominal.noise}}$ is considered. In Fig. 8, curve (b), the SNR_{ADC} is shown when the effects of $P_{\text{nominal.noise}}$ and P_{rn} are both considered. Fig. 9 shows the SNR according to a variation in the resolution bits and amount of jitter in the clock frequency (F_{sampling}). For an ADC with resolution of 14 bits or more, the SNR decreased steeply when the clock jitter was 0.2 ps or more.

C. Bandlimited IF Filter

Ideally, the entire spectrum, except for the bandwidth of the wanted signal containing information as the ADC input signal, should be removed using a filter. In other words, the input signal of an ADC needs a bandlimited desired signal. A band-sampling ADC in a digital-IF receiver application needs a steep bandpass IF filter to serve as a bandlimited filter. In real time, an unwanted signal that is not sufficiently removed by the filter will remain present, as in Fig. 10(a). After this unwanted signal is processed by the sampler, the wanted signal will become distorted due to the overlapping of the surplus spectrum of the unwanted signal, as shown in Fig. 10(b).

After the ADC sampling process, there are two main distortion sources for the ADC output. The first is distortion due to spectrum overlapping by an unwanted signal; the second is distortion of the internal nonlinearity of the ADC, such as spurs. When designing an IF filter, unless unwanted signals can be sufficiently attenuated, distortion due to spectrum overlapping will dominate the ADC output. This can then seriously degrade the SNR and SFDR performance. As such, the attenuation characteristics of an IF filter must be smaller than any spurs caused by an internal nonlinearity of the ADC. In general, the specifications for a bandlimited filter are tighter for receiver applications using a bandpass-sampling ADC rather than an oversampling ADC.

VI. Receiver-Sensitivity Calculation Using ADC-SNR/SFDR

The harmonic distortion of the output of an ADC is induced into the Nyquist band by aliasing those harmonics with a Nyquist or higher frequency. Conventionally, a dithering technique has been used to reduce harmonic distortions. The basic concept is that the addition of wide-band thermal noise to the input of an ADC can randomize the periodic components out of quantization noise, which cause harmonics, thereby reducing the spurious components. However, the amount of

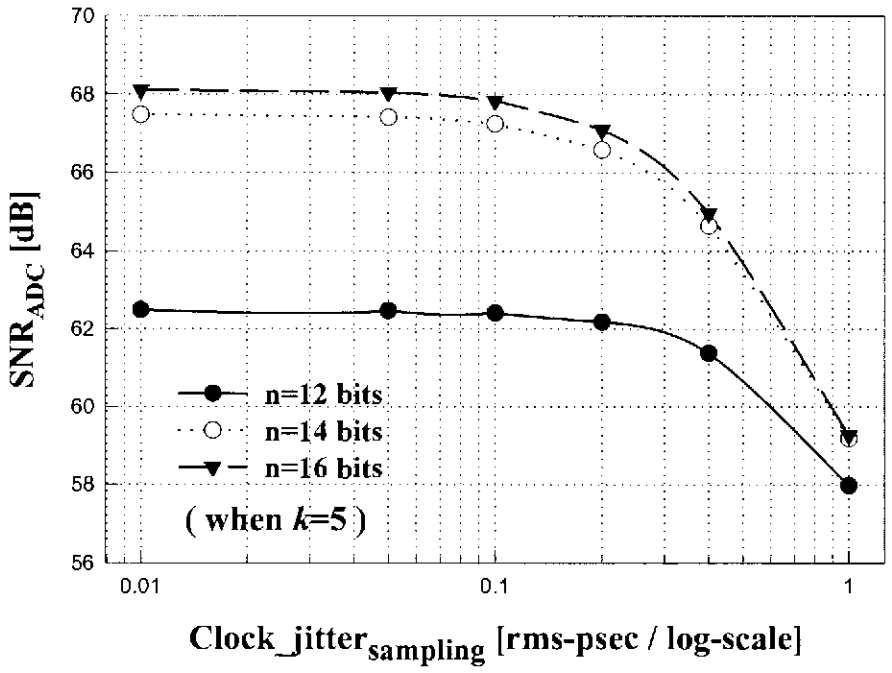


Fig. 9. Relationship between $\mathrm{SNR}_{\mathrm{ADC}}$ and clock jitter.

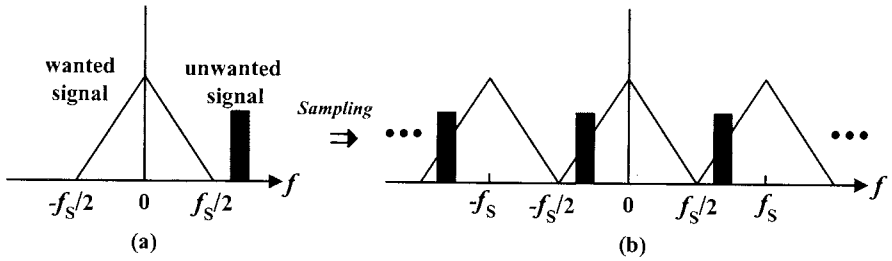


Fig. 10. Spectrum analysis of sampling.

wide-band thermal noise added is an important decision. Generally, the amount of wide-band thermal noise quarantining the maximum SFDR is determined by measurement. Otherwise, the SNR results are affected by the addition of noise power.

In receiver applications using a bandpass-sampling ADC, for receiver sensitivity, the SFDR and SNR must both be carefully considered. Minimum detectable signals (MDSs) due to the SNR and SFDR can be quite different; as such, these two parameters are basically in competition with each other when determining the MDS. This paper used a process that decides the SFDR for the MDS required in the system specifications after determining the MDS according to variations in the ADC-SNR.

The basic block diagram of a digital-IF receiver for UMTS BTS is shown in Fig. 11. The maximum input signal power with the HATA model was calculated as approximately -48.5 dBm. However, the in-band maximum blocker signal power represented in the 3GPP specification is -40 dBm [8]. As such, the RF/IF conversion gain (CG) is expressed (12) because the in-band maximum blocker is stronger than the maximum input power from an antenna.

$$\mathrm{CG[dB]} = \mathrm{FSR}_{\mathrm{ADC}} - \mathrm{Blocker}_{\mathrm{Max}} - \mathrm{Headroom}. \tag{12}$$

Here, the full-scale range of an ADC is expressed by $\mathrm{FSR}_{\mathrm{ADC}}$. The headroom (HD) is considered based on both the peak-to-average-ratio of the transmitter output and a few dB margins related to how much

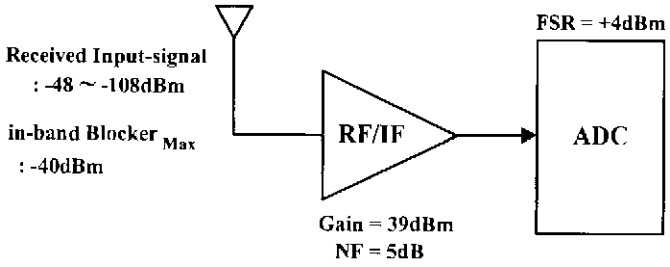


Fig. 11. RF/IF architecture.

$\mathrm{Blocker}_{\mathrm{Max}}$ is located under the FSR of the ADC so as to avoid matching it with the FSR. Also, it should be noted that the HD is increased by 20 log(the number of carriers) in the case of a multicarrier application. This paper assumed the numbers of carriers to be one.

Fig. 12 shows the cascaded SNR of the desired signal for a digital-IF receiver system. The $\mathrm{SNR}_{\mathrm{ADC.out}}$ of the ADC output is represented as the subtraction of the $\mathrm{SNR}_{\mathrm{ADC.loss}}$ due to noises generated in the ADC itself from the $\mathrm{SNRSNR}_{\mathrm{ADC.in}}$ of the desired signal. If the summation of $\mathrm{SNR}_{\mathrm{ADC.out}}$ and $\mathrm{GP}_{\mathrm{despreading}}$, the gain of the spectrum-despreading process of the digital block, is satisfied by the E_b/N_o required in the modem, information with the desired BER can be recovered. Generally, assuming that there is no SNR loss in the digital-block,

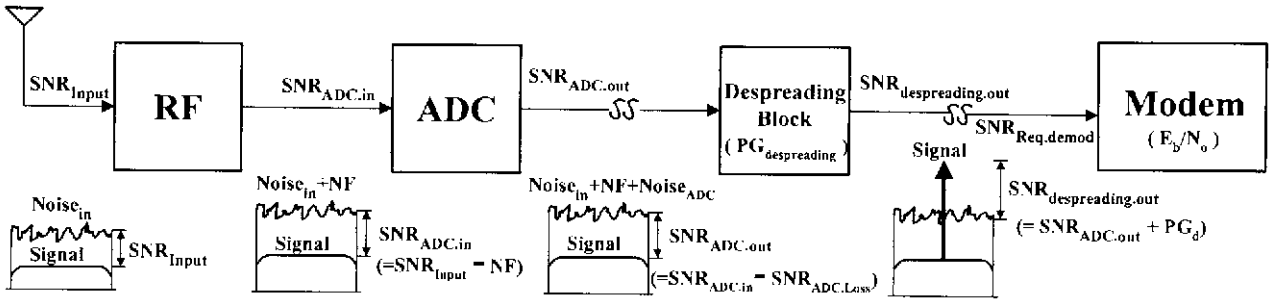


Fig. 12. Cascaded SNR of desired signal.

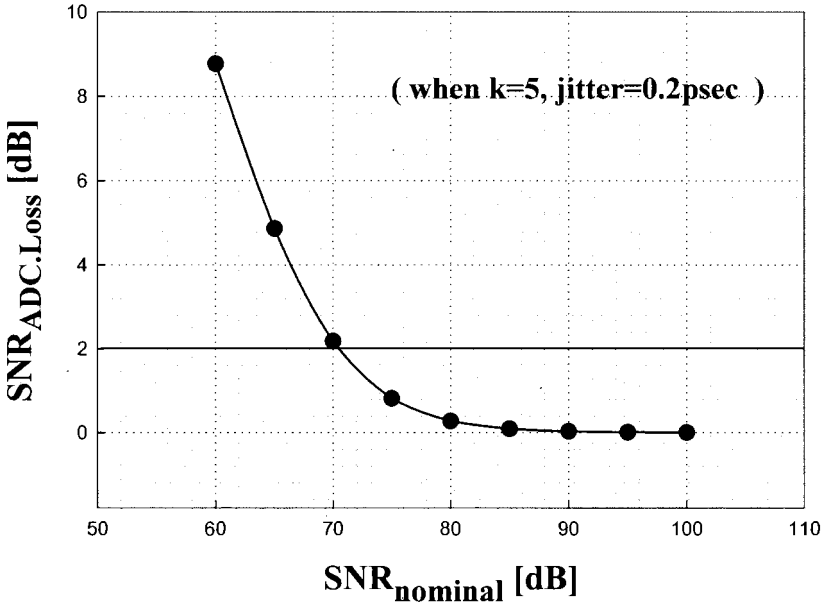


Fig. 13. $\mathrm{SNR_{ADC.Loss}}$ versus $\mathrm{SNR_{nominal}}$ (a) MDS versus channel index. (b) $\mathrm{SFDR_{required}}$ versus channel index.

the MDS can be represented by evaluating the SNR of the desired signal of the receiver input/output

$$\text{MDS [dBm]} = KTB + NF + \frac{E_b}{N_o} - \text{PG}_{\text{despreading}} + \frac{\text{SNR}_{\text{ADC.Loss}}}{(\cong 0)}. \quad (13)$$

The $\mathrm{SNR_{ADC.Loss}}$ can be represented by (14), which is based on the subtraction of P_{rn} from $P_{\text{total.noise}}$

$$\begin{aligned}\text{SNR}_{\text{ADC.Loss}}\ [\text{dB}] &= \text{SNR}_{\text{ADC.in}} - \text{SNR}_{\text{ADC.out}} \\ &= (P_S - P_{rn}) - (P_S - P_{\text{total.noise}}) \\ &= P_{\text{total.noise}} - P_{rn}. \end{aligned} \quad (14)$$

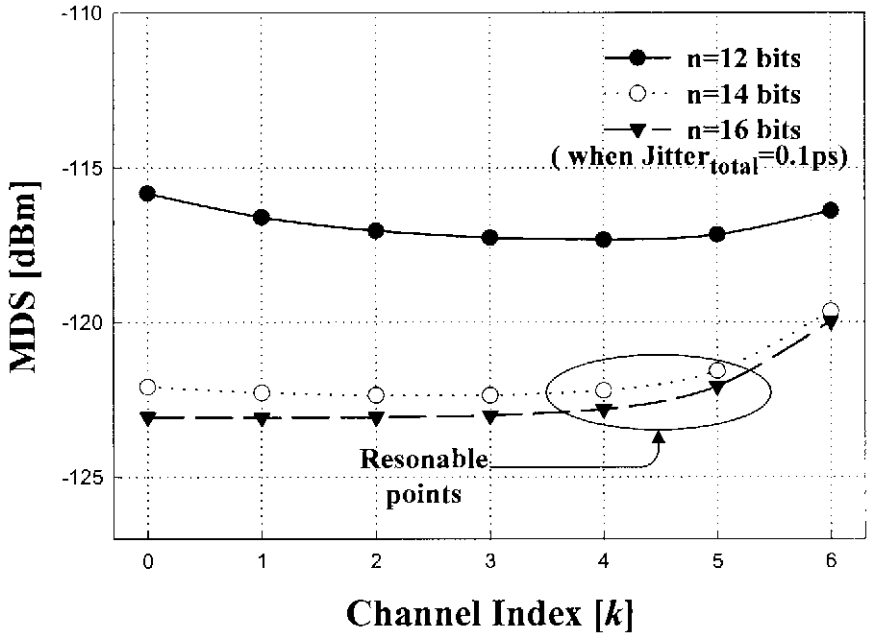
For an ADC used in a conventional receiver architecture that includes AGC loops to improve the receiver's dynamic range, the $\mathrm{SNR_{ADC.Loss}}$ as (13) is nearly zero because P_{qn} is much weaker than P_S. However, in the case of an ADC used in a digital-IF receiver without any AGC loops, in order to neglect the $\mathrm{SNR_{ADC.Loss}}$ during the ADC process, the ADC requires a higher amount of resolution bits than a conventional ADC. These points increase the performance requirements for a band-pass-sampling ADC. However, the tradeoff between the receiver sensitivity and the requirements for an ADC with immature analog-to-digital conversion technology can be utilized if a tolerable ADC/SNR-loss can be allowed.

Fig. 13 shows the $\mathrm{SNR_{ADC.Loss}}$ of an ADC according to the $\mathrm{SNR_{nominal}}$. To approach an $\mathrm{SNR_{ADC.Loss}}$ of zero, as in Fig. 13, the ADC needs an $\mathrm{SNR_{nominal}}$ of 80 dB or more with a resolution of 16 bits or more. For example, assuming an E_b/N_o of 5 dB, $\mathrm{GP_{despreading}}$ of 25 dB, NF of 5 dB, KTB of -108 dBm (-174 dBm $+ 10\log$BW) and MDS of -121 dBm or less, the $\mathrm{SNR_{ADC.Loss}}$ will be 2 dB or less. In this case, an $\mathrm{SNR_{nominal}}$ of 70 dB or more is needed with a resolution of 14 bits or more. Accordingly, this example shows the satisfaction of the MDS specifications based on sacrificing the sensitivity due to immature analog-to-digital conversion technology. Also, in the real-time design of a base-station receiver, the consideration of parameters such as the user capacity, cell coverage, etc., will also influence the receiver sensitivity. As a result, the margin of $\mathrm{SNR_{ADC.Loss}}$ satisfying the MDS can be reduced.

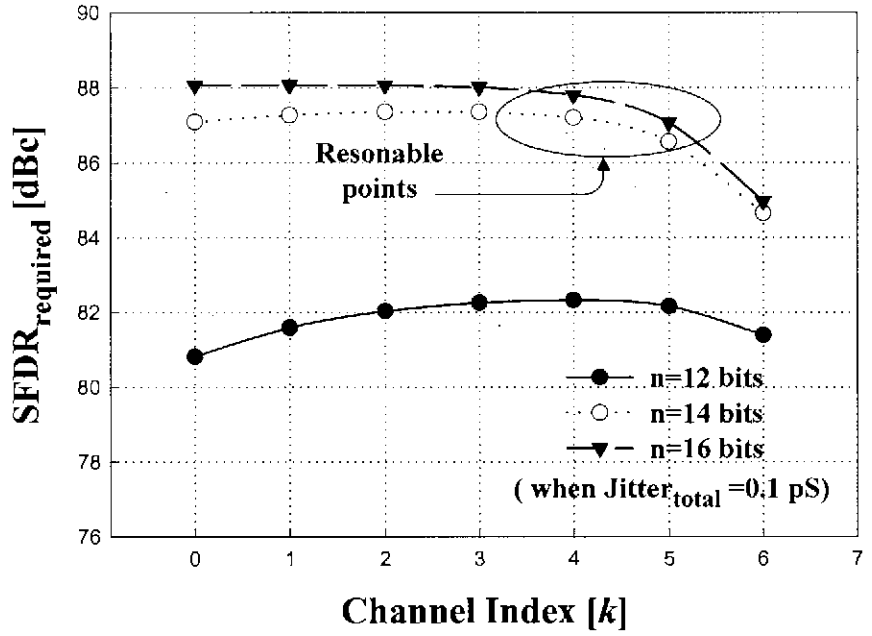
When assuming an FSR of 4 dBm and HD of 5 dB, the CG is equal to 39 dB. From the ADC-SNR, the MDS of a digital-IF receiver can be described by (15)

$$\text{MDS [dBm]} = \text{FSR-CG-SNR}_{\text{ADC}} + \frac{E_b}{N_0} - \text{PG}_{\text{despreading}}. \quad (15)$$

In (11), the $\mathrm{SNR_{ADC}}$ is not a nominal SNR offering the maximum SNR, but rather the real SNR. The value of $\mathrm{SNR_{ADC}}$ is influenced by F_S, F_{IF}, the jitter effect, CG, and P_{rn} containing the RF/IF gain and the system NF. The CNR is defined as the carrier-to-noise ratio for the proper demodulation according to the modulation scheme. For



(a)



(b)

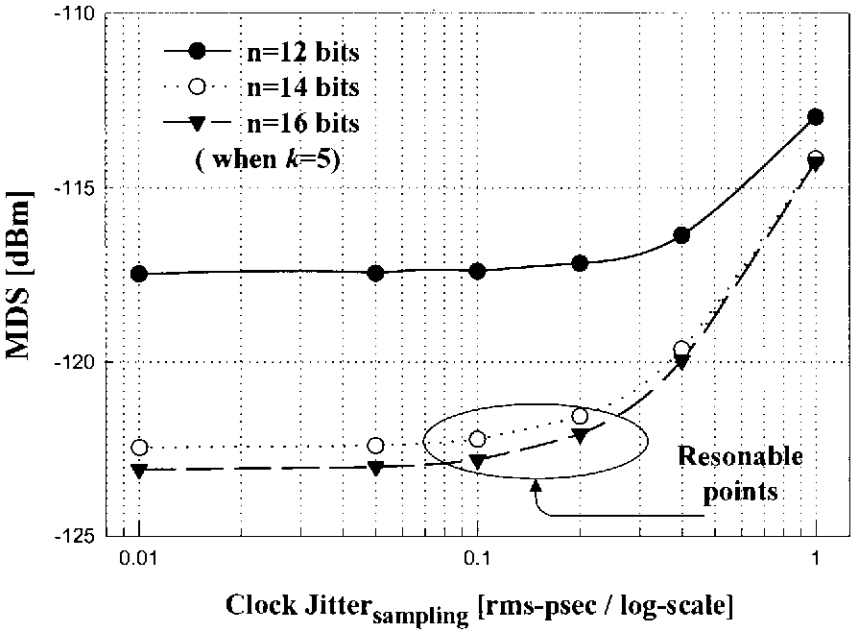
Fig. 14. MDS/SFDR$_{\mathrm{required}}$ versus channel index. (a) MDS versus clock jitter. (b) SFDR$_{\mathrm{required}}$ versus clock jitter.

example, when an ADC with a resolution of 14 bits is used along with an SNR of 66.6 dB, the MDS becomes -121.2 dBm with an HD of 5 dB, CNR of -20 dB, NF of 5 dB, data rate of 12.2 kbps, F_{IF} of 92.16 MHz, F_S of 122.88 MHz, and jitter of 0.2 ps. These values satisfy the minimum sensitivity of UMTS-BTS. In Fig. 14(a), the receiver MDS is plotted according to the channel index of k with a variation in the resolution bits. To satisfy the minimum reference sensitivity of a UMTS base station, an ADC is required for a channel index of five or less and resolution of 14 bits or more. In this case, F_{s} and F_{IF}, as determined by a channel index of k, are 122.88 and 96.12 MHz, respectively.

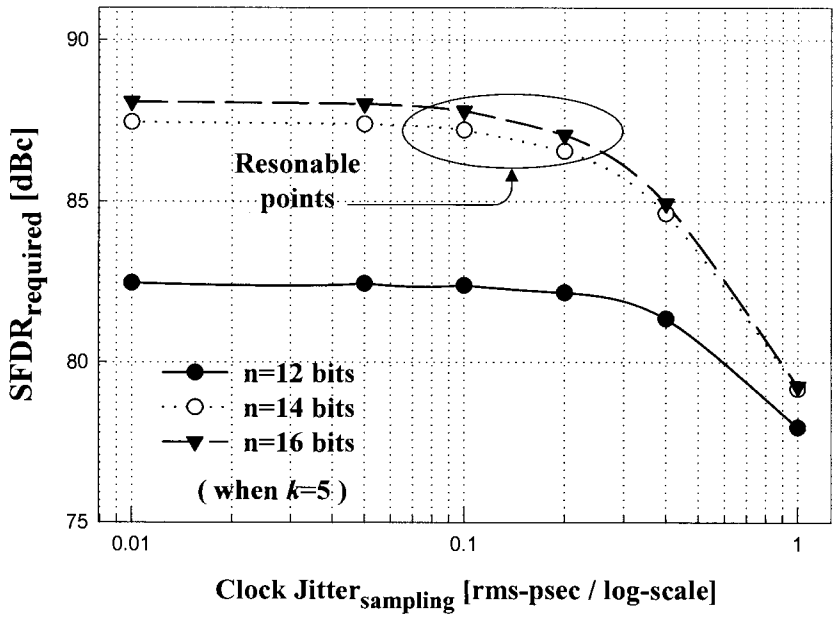
The spurious power level in the desired bandwidth must be considered along with the possibility of a limitation in receiver sensitivity in contrast to limitation due to the SNR. In (16), the SFDR$_{\mathrm{required}}$ is expressed based on the MDS in (15). Here, the RF/IF path gain is represented by the *Gain*. The *CIR* in the multichannel system is defined by the ratio of the carrier to the interference

$$\mathrm{SFDR}_{\mathrm{required}}[\mathrm{dBc}] = \mathrm{FSR}_{\mathrm{ADC}} - \mathrm{MDS} - \mathrm{Gain} + \mathrm{CIR}. \qquad (16)$$

For example, assuming an FSR of 4 dB, MDS of -121 dBm, gain of 32 dB, NF of 5 dB, and CIR of 0 dB, the SFDR$_{\mathrm{required}}$ is calculated as 78.2 dBc. In Fig. 14(b), the receiver SFDR$_{\mathrm{required}}$ is plotted according to the channel index of k with a variation in the resolution bits. To satisfy the minimum reference sensitivity of -121 dBm, the receiver SFDR$_{\mathrm{required}}$ is required to be about 86.5 dBc or more.



(a)



(b)

Fig. 15. MDS/xs $\mathrm{SFDR}_{\mathrm{required}}$ versus clock jitter.

TABLE I
IIP3, OIP3, MAXIMUM OUTPUT-SIGNAL OF RF/IF SECTION

Components	IIP3 [dBm]	OIP3 [dBm]	Output-Signal (Gain) [dBm]
RF Amp	10	35	-15 (+25)
RF Filter	35	29	-21 (-6)
RF Mixer	29	23	-27 (-6)
IF Amp	23	49	-1 (+26)
IF Filter	49	49	-1 (0)
(When, HD=5dB, FSR=4dBm, Blocker=-40dBm)			

Generally, the SNR/SFDR of an ADC is susceptible to jitter from both the clock and the ADC itself. This effect is shown in Fig. 15. In Fig. 15(a) the receiver MDS is plotted according to the clock $\mathrm{jitter}_{\mathrm{sampling}}$ with a variation in the resolution bits assuming that the internal jitter of the ADC is zero. To satisfy the MDS of a UMTS base station, an ADC is required with a total jitter of 0.2 ps or less and a resolution of 14 bits or more. In Fig. 15(b), the receiver $\mathrm{SFDR}_{\mathrm{required}}$ is plotted according to the clock $\mathrm{jitter}_{\mathrm{sampling}}$ with a variation in the resolution bits. As such, the limitation of the clock jitter was found to satisfy the MDS and $\mathrm{SFDR}_{\mathrm{required}}$.

VII. LINEARITY REQUIRED IN RF/IF STAGE

The receiver spurious performance is influenced not only by the SFDR and dither of an ADC but also by the linearity of the RF/IF components. In the receiver design, the third-order intercept (IIP3) is an important measure in determining the linearity of the performance

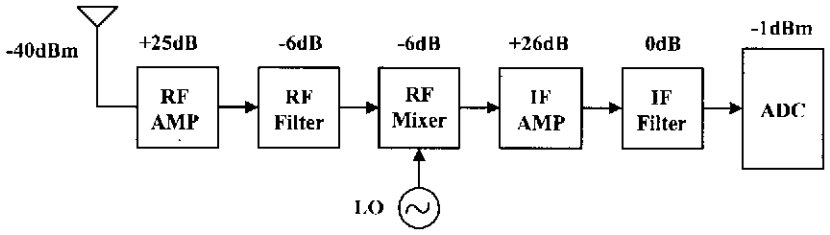


Fig. 16. RF/IF section of digital-IF receiver.

relative to an increasing signal power level. The IIP3 is shown in (17) [5]

$$\text{IIP}_3\ [\text{dBm}] = 1.5P_{\text{signal}} - 0.5P_{\text{IMD}}. \tag{17}$$

Here, P_{signal} is a two-tone power that causes the intermodulation product (IMD), while P_{IMD} is the power of the IMD. Fig. 16 shows a basic block diagram of the RF/IF section of a digital-IF receiver for UMTS-BTS. Assuming that the total spurious performance is 100 dB or more, the IIP3 for each stage can be calculated using (17) and the results are shown in Table I. The input power level of an ADC is determined by the difference between the FSR and the HD, -1 dBm. The values of IIP3 and gain in Table I are optimized for real-time implementation.

VIII. Conclusion

The rapid development of digital wireless systems has led to a need for multistandard multichannel RF receivers. This paper selected a digital-IF receiver architecture for such applications. Since this receiver architecture does not include an AGC loop, it requires an ADC with a high dynamic range because the blockers are not attenuated. Also, the channel selection process is carried out entirely using digital filters of digital blocks.

This paper analyzed the relationship between the performance of a bandpass-sampling ADC and the requirements of a digital-IF receiver for a wide-band CDMA base station. Therefore, the ADC SNR, the derivation of the receiver sensitivity using the ADC-SNR/SFDR, the effect of the ADC clock jitter and receiver linearity, and the relationship between the receiver IF and the ADC sampling frequency were all covered. The design of a WCDMA digital-IF receiver that can support a multistandard multichannel application involves many challenges to achieve a comparable performance with conventional ADCs. However, a tradeoff between the receiver sensitivity and the requirements of an ADC with immature analog-to-digital conversion technology can be utilized if a tolerable ADC-SNR loss is allowed. Furthermore, since the real-time design of a base-station receiver must also consider such parameters as user capacity and cell coverage, etc., this will also influence the receiver sensitivity. The requirements of an ADC are thus much tighter due to these effects. Moreover, the noise sources generated by a multiuser multichannel application also lead to further degradation of the receiver sensitivity.

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On the SER and Spectral Analyses of A-Law Companded Multicarrier Modulation

Xianbin Wang, T. T. Tjhung, and Yiyan Wu

***Abstract*—A peak-to-average power ratio (PAPR) reduction technique based on A-law companding is proposed for a multicarrier modulation (MCM) system. The symbol error rate (SER) and spectral property of the companded MCM system are investigated. The SER and spectral performance of the proposed system are also compared with uncompanded MCM system.**

***Index Terms*—A-law companding, multicarrier modulation (MCM), peak-to-average power ratio (PAPR).**

I. Introduction

Multicarrier modulation (MCM), also known as orthogonal frequency-division multiplexing or digital multitone, has several properties that make it an attractive modulation scheme for high-data-rate transmission, like immunity to intersymbol interference and impulse noise, low complexity, and high spectral efficiency. Since an MCM signal is the summation of a large number of subcarriers, the amplitude of the signal can be approximated to be Gaussian distributed, indicating the signal has a very large peak-to-average power ratio (PAPR). Recently, a simple yet effective μ-law companding technique was used [1]–[3] to reduce the high PAPR. In this paper, a PAPR reduction technique based on A-law companding is proposed and studied for an MCM system.

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