Ahmad GHANAATIAN-JAHROMI[1], Adib ABRISHAMIFAR[1], Ali MEDI[2]

Iran University of Science and Technology (1), Sharif University of Technology (2)

A novel voltage-to-voltage logarithmic converter with high accuracy

***Abstract**. A novel BiCMOS voltage-to-voltage converter with logarithmic characteristics and very high accuracy is presented. The relationship between the emitter current and the base-emitter voltage in bipolar transistors is used to realize the logarithmic function. With 1.8 supply voltage, the total power consumption is less than 15.75 mW and a Log error of < -36dB is shown in the ADS simulations. Compared to the other method in the literature, very better accuracy in logarithm calculation is achieved. The proposed method can be used in arithmetical operation circuits like analog processors.*

***Streszczenie.** Przedstawiono nowy przetwornik logarytmujący w technologii BiCMOS. Do realizacji funkcji logarytmującej użyto zależności między prądem emitera i napięciem baza-emiter w tranzystorze bipolarnym. Przy napięciu zasilającym 1.8V pobór mocy był mniejszy niż 15.75 mW a błąd logarytmowania był mniejszy niż -36dB. W porównaniu z podobnymi układami prezentowanymi w literaturze Osiągnięto lepszą dokładność. (**Przetwornik logarytmujący o dużej dokładności**).*

Keywords: Arithmetical circuits; Logarithmic Amplifier; Logarithmic converter.
Słowa kluczowe: wzmacniacz logarytmujący, układy arytmetyczne.

Introduction

Logarithmic functions are widely used in instrumentation telecommunications, medical equipments, radar receivers and arithmetical operation circuits [1-3]. Logarithmic circuits need to have high input dynamic range to compress the large amplitude of the signals in the radar receivers input, high accuracy for arithmetical operation functions and low power consumption in order to be useful in communication circuits [1]. A square-law characteristic in strong inversion of MOS transistors cannot lead to logarithmic function while the bipolar transistors behavior can be used to generate it easily. On the other hand, good performance bipolar transistors are not available in CMOS-based technologies [4]. Moreover, utilizing MOS transistors in the weak inversion region which has the exponential behavior will reduce the input dynamic range significantly.

Several approaches of generating logarithmic functions for different applications have been proposed in the literature which are discussed here. Fig. 1 shows the progressive–compression structure which was used in [5], [6]. In this approach several auxiliary voltages are created using series of linear-limit amplifiers. A current proportional to the voltage of each stage is generated by taking advantage of a transconductance element. The summation of all these currents with proper transconductance ratio can approximate the logarithmic function piecewise. With a little systematic difference with the previous method, the parallel amplification type circuit was used in [7],[8]. Fig. 2 presents the system diagram of this approach. High symmetry in different path which is lead to the good phase and group delay matching is the strength of this method, while its input dynamic range is lower than the previous on [1].

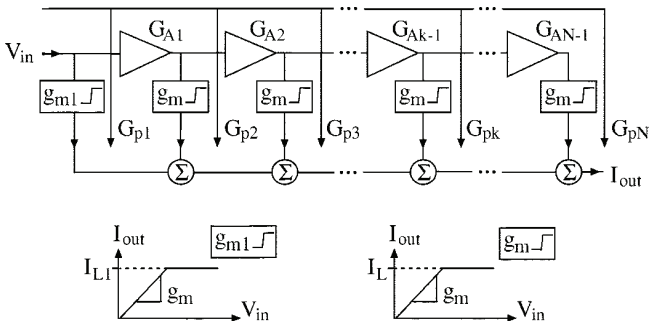

Fig.1. Progressive-compression topology

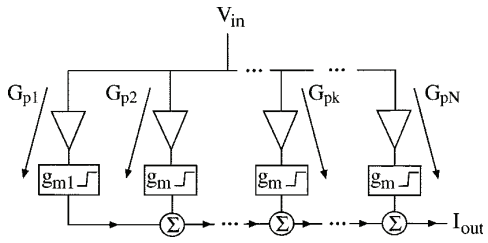

Fig.2. Parallel amplification topology

By taking advantages of the above approaches combination, which are the subdivisions of parallel-summation technique, [1] got better properties in approximating logarithmic function piecewise. All reviewed approaches which are based on piecewise approximation, can be employed where high input dynamic range compression is needed but are not useful in basic arithmetic function circuits as they are complicated while suffer from poor accuracy.

Motivated by the need for good accuracy, some other techniques like Taylor series [9],[10] and current conveyors [11] were utilized to attain logarithmic and exponential behaviors, but none of them could be realized with a simple structure. However, utilizing a single MOS transistor with gate-to-substrate biasing technique in [2] can solve the complicated circuit and accuracy problems simultaneously, but a very poor input dynamic range of about 1.5uA makes it impractical.

In this paper, a simple circuit based on intrinsic exponential characteristic of the bipolar devices is proposed. At first a MOS transistor is used in order to convert voltage to current and then logarithmic characteristic is obtained by injecting the current to a bipolar transistor. Simulation results in ADS software using TSMC 0.18um BiCMOS process models confirm the well acceptable accuracy for arithmetic functions applications. In section 2 the basis of logarithmic behaviors will be considered and completed with the circuit design procedure and the simulation results in section 3. Concluding remarks are provided in section 4.

The basis of logarithmic behavior

Exponential function can be obtained via the relationship between emitter current and base-emitter voltage in a bipolar transistor.

$$I_E = I_S\left(e^{\frac{\eta V_{BE}}{V_t}} - 1\right) \quad (1)$$

Therefore, logarithmic characteristics can be achieved by a little change in (1).

$$V_{BE} = \frac{V_t}{\eta}\ln\left(\frac{I_E}{I_S}\right) \quad while \quad I_E \gg I_S \quad (2)$$

(2) can be written as below, too.

$$V_{BE} = \frac{V_t}{\eta}\ln I_E - \frac{V_t}{\eta}\ln I_S = a\ln I_E - b \quad (3)$$

So a linear relationship between V_{BE} and $\ln(I_E)$ is available. Thus far logarithmic current to voltage converter is available by a single bipolar transistor; however, voltage to voltage converter is the final goal. In this case, a voltage to current converter is also needed. This can be done by means of a single MOS transistor. Because of the logarithm function characteristics, a square-law behavior in strong inversion region of the MOS elements cannot destroy logarithmic relationship.

$$I_D = k\left(V_{gs} - V_T\right)^2 \quad (4)$$

Using (4) instead of I_E in (3):

$$V_{BE} = a\ln\left[k\left(V_{gs} - V_T\right)^2\right] - b = 2a\ln\left[\sqrt{k}\left(V_{gs} - V_T\right)\right] - b$$
$$= 2a\ln\left(\sqrt{k}\right) + 2a\ln\left(V_{gs} - V_T\right) - b = p\ln\left(V_{gs} - V_T\right) + q \quad (5)$$

Using proper dimensions (w/l) for MOS element may cause the q to become zero while it can be made zero by taking advantage of DC level shifting in the output stage, too. In this section, it is demonstrated that logarithmic converter can be realized using a MOS element for voltage to current converting and a bipolar transistor for logarithmic behaving.

Circuit design and simulation results

Circuit-level implementation of the proposed method is presented here in Fig. 3.

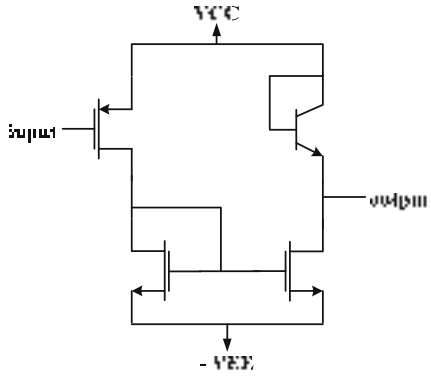

Fig.3. Simple logarithmic converter

Logarithmic behavior in the output voltage can be achieved through feeding the current which is in proportion to the input voltage, into a bipolar transistor. The simple topology has two issues discussed below. The first one is about the linear voltage to current converting which is not accessible in this case and can be obtained if the input voltage is equaled to $(V_{gs}\text{-}V_T)$. Furthermore in this technology, the P-channel transistor characteristics are not as well as the N-channel. As the accurate square-law behavior is needed for the accurate logarithmic function according to mathematical equations, The NMOS transistor is a better choice for the circuit input actually.

The second issue is the low output dynamic range. Big changes in the collector current value will cause low alteration in the base-emitter voltage due to the exponential relationship. The lower output dynamic range requires higher gain for the next stage to achieve logarithmic converter. The problems are solved in the new topology which is depicted in Fig. 4. Another stage should be added for amplifying and level shifting. Fig. 5 shows the final circuit.

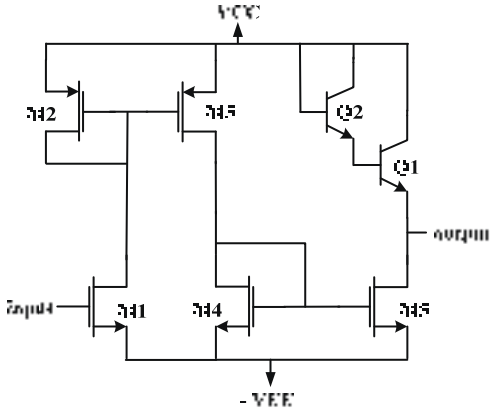

Fig.4. Repaired Logarithmic converter

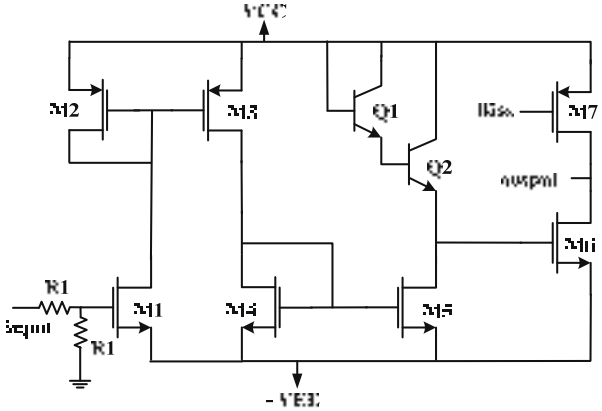

Fig.5. Final Circuit for logarithmic converter

To enclose the operation of the proposed circuit it should be expressed that the logarithm of all positive numbers can be calculated using the logarithm of numbers between 1 to e. (6) shows how all positive numbers can be mapped in to the [1,e] zone.

$$x = y.e^k \Rightarrow \ln(x) = \ln(y) + k \quad (6)$$

If x is a real positive number and k is an integer, y will be a real number between 1 and e. So logarithm of y is sufficient to calculate the logarithm of x. For this reason the input dynamic range of the proposed circuit is determined between 1 and e. The equaled resistors are used to divide the input voltage by two, because the positive supply voltage of 1.3 volt is not enough to support the dynamic range of [1,e]. Also, as the threshold voltage of the

transistors in the used technology is about 0.5 volt, the minus supply voltage is fixed to -0.5 volt to recoup the input voltage. It is manifestly shown in (7).

$$(7)\quad I_d \ \alpha\ (v_{gs}-v_T) \rightarrow I_d \ \alpha\ (v_A+v_{EE}-v_T) \xrightarrow{v_{ss}=v_T} I_d \ \alpha\ v_A \rightarrow I_d \ \alpha\ v_{in}$$

Fig. 6 shows the simulation results of proposed circuit and an ideal logarithmic converter in 100MHz.

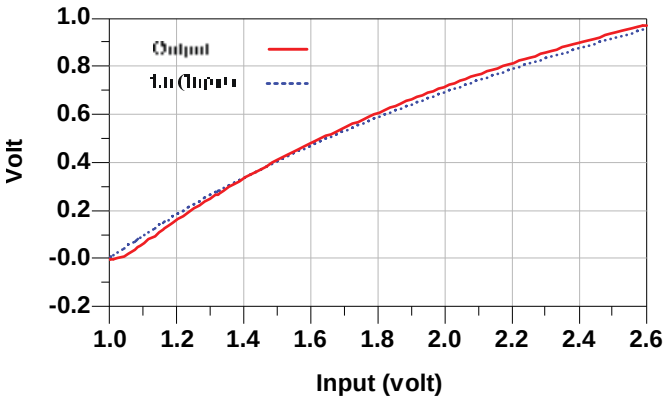

Fig.6. Simulation result of proposed circuit and ideal logarithmic converter in 100MHz

Time domain simulation is depicted in Fig. 7 to verify the proper operation of the designed circuit.

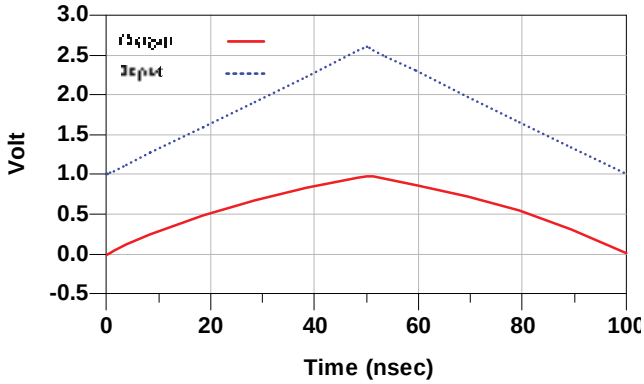

Fig.7. Input and output of the proposed logarithmic converter

The behavior of the proposed logarithmic converter over different frequencies will be changed. It can have a different rise and fall shape and of course it is not unexpected because of the accumulated charges in the base of bipolar devices and short channel effects in the MOS elements. Fig. 8 demonstrates the output in 200MHz and 400MHz.

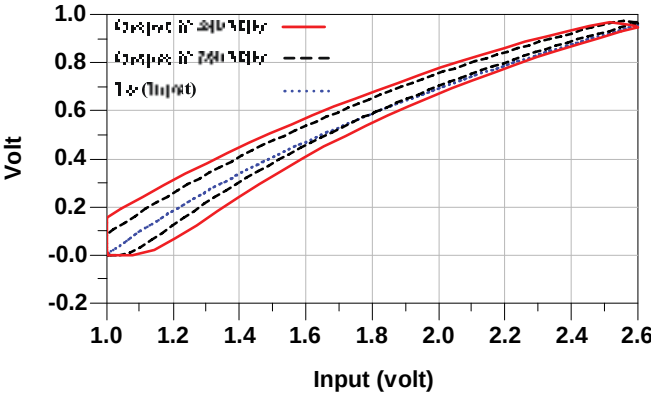

Fig.8. Proposed circuit output in two different frequencies

Moreover, Fig. 8 shows the Log error increases as the frequency goes up. Thus, Fig. 9 is provided to report the details.

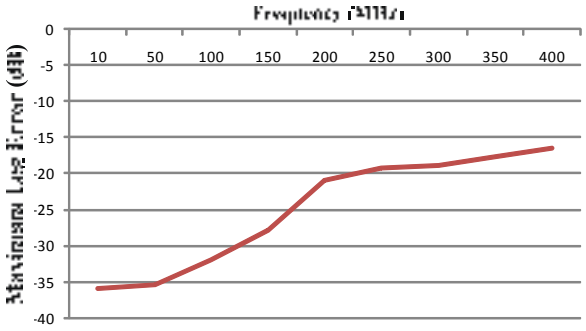

Fig.9. Log error of proposed circuit

Very low Log error especially before 100MHz shows that the presented approach is very promising for arithmetical applications. Table 1 shows a comparison of this work with some other logarithmic amplifiers.

Conclusion

In this paper, a novel voltage to voltage logarithmic converter for arithmetical circuits was proposed. The idea was originated from the intrinsic characteristics of bipolar transistors. Very low error in logarithm calculation which is so important for arithmetical circuits, show the strength of the proposed. Additionally, a method of mapping the whole positive real numbers in to the (1, e) zone was used to show that the large input dynamic range is not necessary.

Table 1. This work and some other logarithmic amplifiers characteristics

	[1]	[9]	[12]	This work
Technology	35GHz Silicon Bipolar	0.25um CMOS	0.35um CMOS	0.18um BiCMOS
Technique	Piecewise approximation	Taylor series	Taylor series	Bipolar intrinsic Behavior
Supply voltage	-5 V	1.5 V	1.5 V	-0.5 v , 1.3 V
power	0.75 W	0.8 mW	0.8 mW	15.75 mW
Error @ low Freq	2 dB	0.5 dB	0.5 dB	-36 dB
Applications	Radar Input Stage	Arithmetical circuit, AGC	Arithmetical circuit, AGC	Arithmetical circuit

REFERENCES

[1] Chris D. Holdenried, James W. Haslett, John G. McRory, R. Douglas Beards, and A. J. BergsmaJ. A DC–4-GHz True Logarithmic Amplifier: Theory and Implementation, *IEEE Journal of Solid-State Circuits,* Vol. 37, No. 10, October 2002.

[2] Sanchi Harnsoongnoen, Chiranut Sa-ngiamsak, Poonsak Intarakul and Rardchawadee Silapunt, "Logarithmic and Antilogarithmic Circuit with Gate-to-Substrate Biasing Technique", *ITC-CSCC*, 2008.

[3] R. F. Wolffenbuttel, Digitally Programmable Accurate Current Source for Logarithmic Control of The Amplification or Attenuation in again Cell, *IEEE Journal of Solid-State Circuit*, Vol.23, pp. 767-773, 1988.

[4] A. B. Grebene, *Bipolar and MOS integrated Circuit Design, John Wiley & Sons*, New York, 1984.

[5] B. Gilbert, "Synchronous logarithmic amplifier," *U.S. Patent 5 298 811*, Mar. 29, 1994.

[6] A. Garskamp, "Logarithmic amplifier with sequentially limiting amplifier stages," *U.S. Patent 5 049 829*, Sept. 17, 1991.

[7] K. Kimura, "Logarithmic amplifying circuit based on the bias-offset technique," U.S. Patent 5 506 537, Apr. 9, 1996.

[8] F. W. Olsen and E. J. Tasillo, "Psuedo logarithmic step adder," *U.S. Patent 5 221 907*, June 22, 1993.

[9] Quoc-hoang duong, T.kien nguyen and Sang-gug lee, CMOS Exponential Current-to-Voltage Circuit Based on Newly Proposed Approximation Method, *ISCAS*, 2004.

[10] Carlos A. De La Cruz-Blas and Antonio Lopez-Martin, Compact Power-Efficient CMOS Exponential Voltage-to-Voltage Converter, *ISCAS* 2006.

[11] F. Bergouignan, N. Abouchi, R. Grisel, G. Caille, J. Caranana, Designs Of A Logarithmic and Exponential Amplifiers Using Current Conveyors, *ICECS* 1996.

[12] Wci hsing Liii, Clieng-Chicli Clieilg and Shcn-I tian TA, Realisation of exponential V-I converter using composite NMOS transistors, *Electronics Letters* 6th January 2000 Val. 36 No. I.

***Authors**: Ahmad Ghanaatian-Jahromi, Electrical Department, Iran University of Science and Technology, Tehran, Iran, E-mail: aghanaatian@ee.iust.ac.ir; Prof Adib Abrishamifar, Electrical Department, Iran University of Science and Technology, Tehran, Iran, E-mail: abrishamifar@iust.ac.ir; Prof Ali Medi, Electrical Department, Sharif University of Technology, Tehran, Iran, E-mail: Medi@sharif.edu.*

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